Title (en)
FIELD-PROGRAMMABLE LOGIC GATE ARRANGEMENT

Title (de)
FELDPROGRAMMIERBARE LOGIK-GATTER-ANORDNUNG

Title (fr)
DISPOSITIF À PORTES LOGIQUES PROGRAMMABLE PAR L'UTILISATEUR

Publication
EP 2801154 A1 20141112 (DE)

Application
EP 12704770 A 20120215

Priority
EP 2012052549 W 20120215

Abstract (en)
[origin: WO2013120516A1] The invention relates inter alia to a field-programmable logic gate arrangement (10). According to the invention, a dual-port or multi-port memory chip (20) having a predetermined number of ports that permit a parallel interrogation of the memory chip (20) and a read-out device (30) are provided. Said read-out device is suitable for reading out in parallel memory cells of the dual-port or multi-port memory chip (20) at at least two ports of the memory chip (20), for comparing in parallel the memory contents (I(A1), I(A2)) emitted at the at least two ports with a predetermined memory content (I-1, I-n) and, when the memory contents match, for emitting a result signal (S1-S4) signalling the match and/or the corresponding memory cell address of the memory cell having the predetermined memory content (I-1, I-n).

IPC 8 full level
H03K 19/177 (2006.01); **G06F 7/02** (2006.01); **H03K 5/22** (2006.01)

CPC (source: EP)
H03K 5/22 (2013.01); **H03K 19/17728** (2013.01); G06F 7/02 (2013.01)

Citation (search report)
See references of WO 2013120516A1

Designated contracting state (EPC)
AL AT BE BG CH CY CZ DE DK EE ES FI FR GB GR HR HU IE IS IT LI LT LU LV MC MK MT NL NO PL PT RO RS SE SI SK SM TR

DOCDB simple family (publication)
WO 2013120516 A1 20130822; BR 112014020003 A2 20170620; BR 112014020003 A8 20170711; CN 104115402 A 20141022; CN 104115402 B 20170315; EP 2801154 A1 20141112; RU 2014137144 A 20160410

DOCDB simple family (application)
EP 2012052549 W 20120215; BR 112014020003 A 20120215; CN 201280069650 A 20120215; EP 12704770 A 20120215; RU 2014137144 A 20120215