

Title (en)  
FIELD-PROGRAMMABLE LOGIC GATE ARRANGEMENT

Title (de)  
FELDPROGRAMMIERBARE LOGIK-GATTER-ANORDNUNG

Title (fr)  
DISPOSITIF À PORTES LOGIQUES PROGRAMMABLE PAR L'UTILISATEUR

Publication  
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Application  
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Priority  
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Abstract (en)  
[origin: WO2013120516A1] The invention relates inter alia to a field-programmable logic gate arrangement (10). According to the invention, a dual-port or multi-port memory chip (20) having a predetermined number of ports that permit a parallel interrogation of the memory chip (20) and a read-out device (30) are provided. Said read-out device is suitable for reading out in parallel memory cells of the dual-port or multi-port memory chip (20) at at least two ports of the memory chip (20), for comparing in parallel the memory contents (I(A1), I(A2)) emitted at the at least two ports with a predetermined memory content (I-1, I-n) and, when the memory contents match, for emitting a result signal (S1-S4) signalling the match and/or the corresponding memory cell address of the memory cell having the predetermined memory content (I-1, I-n).

IPC 8 full level  
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CPC (source: EP)  
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