Title (en)

METHOD OF ONO INTEGRATION INTO LOGIC CMOS FLOW

Title (de)

VERFAHREN ZUR ONO-INTEGRATION IN EINE LOGISCHE CMOS-STRÖMUNG

Title (fr)

PROCÉDÉ D'INTÉGRATION ONO DANS UN FLUX CMOS LOGIQUE

Publication

EP 2831918 A4 20151118 (EN)

Application

EP 13767491 A 20130313

Priority

- US 201213434347 A 20120329
- US 2013030874 W 20130313

Abstract (en)

[origin: WO2013148196A1] An embodiment of a method of integration of a non-volatile memory device into a logic MOS flow is described. Generally, the method includes: forming a pad dielectric layer of a MOS device above a first region of a substrate; forming a channel of the memory device from a thin film of semiconducting material overlying a surface above a second region of the substrate, the channel connecting a source and drain of the memory device; forming a patterned dielectric stack overlying the channel above the second region, the patterned dielectric stack comprising a tunnel layer, a charge-trapping layer, and a sacrificial top layer; simultaneously removing the sacrificial top layer from the second region of the substrate, and the pad dielectric layer from the first region of the substrate; and simultaneously forming a gate dielectric layer above the first region of the substrate and a blocking dielectric layer above the charge-trapping layer.

IPC 8 full level

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CPC (source: CN EP KR)

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Citation (search report)

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- See also references of WO 2013148196A1

Designated contracting state (EPC)

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