

Title (en)

INTEGRATION OF NON-VOLATILE CHARGE TRAP MEMORY DEVICES AND LOGIC CMOS DEVICES

Title (de)

INTEGRATION NICHTFLÜCHTIGER LADUNGSSPEICHERVORRICHTUNGEN UND LOGISCHER CMOS-VORRICHTUNGEN

Title (fr)

INTÉGRATION DE DISPOSITIFS DE MÉMOIRE NON VOLATILE À PIÉGEAGE DE CHARGES ET DISPOSITIFS CMOS LOGIQUE

Publication

EP 2831919 A4 20160323 (EN)

Application

EP 13769241 A 20130318

Priority

- US 201213436878 A 20120331
- US 2013032777 W 20130318

Abstract (en)

[origin: WO2013148393A1] An embodiment of a method of integrating a non-volatile memory device into a logic MOS flow is described. Generally, the method includes: forming in a first region of a substrate a channel of a memory device from a semiconducting material overlying a surface of the substrate, the channel connecting a source and a drain of the memory device; forming a charge trapping dielectric stack over the channel adjacent to a plurality of surfaces of the channel, wherein the charge trapping dielectric stack includes a blocking layer on a charge trapping layer over a tunneling layer; and forming a MOS device over a second region of the substrate.

IPC 8 full level

H01L 29/792 (2006.01); **B82Y 10/00** (2011.01); **H01L 21/28** (2006.01); **H01L 27/115** (2006.01); **H01L 29/66** (2006.01); **H01L 29/06** (2006.01); **H01L 29/78** (2006.01)

CPC (source: CN EP KR)

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Citation (search report)

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- [Y] US 2008293207 A1 20081127 - KOUTNY JR WILLIAM W C [US], et al
- See references of WO 2013148393A1

Designated contracting state (EPC)

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