

Title (en)

METHOD FOR PRODUCING A DPA-RESISTANT LOGIC CIRCUIT

Title (de)

VERFAHREN ZUR HERSTELLUNG EINER DPA-RESISTENTEN LOGISCHEN SCHALTUNG

Title (fr)

PROCÉDÉ DE FABRICATION D'UN CIRCUIT LOGIQUE RÉSISTANT AUX ATTAQUES DPA

Publication

EP 2842066 A1 20150304 (DE)

Application

EP 13717247 A 20130412

Priority

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- EP 2013057651 W 20130412

Abstract (en)

[origin: WO2013160122A1] The invention relates to a method for producing a logic circuit, in particular an application-specific integrated circuit or ASIC. A description of the logic circuit is formulated (2) in a hardware description language and then converted (3) into a description of a corresponding physical circuit, i.e. into a netlist, using a conversion program, i.e. a synthesis tool, said description consisting at least largely of standard cells (S1, S2, S3, S4, S5). During the conversion process, the standard cells (S1, S2, S3, S4, S5) which are used in the netlist are replaced (4) with standard cell (S1, S2, S3, S4, S5) versions (vS1, vS2, vS3, vS4, vS5) which have a correspondingly balanced power dissipation. Spying on a mode of operation of the circuit by analyzing a power consumption of the circuit is thus advantageously hindered or prevented, in particular in security-relevant circuits.

IPC 8 full level

G06F 17/50 (2006.01)

CPC (source: EP US)

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Citation (search report)

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DOCDB simple family (publication)

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