

Title (en)
MASK LEVEL REDUCTION FOR MOFET

Title (de)
MASKIERUNGSSTUFENREDUZIERUNG FÜR MOFET

Title (fr)
RÉDUCTION DU NIVEAU DE MASQUE POUR UN TRANSISTOR À EFFET DE CHAMP À SEMI-CONDUCTEUR À OXYDE MÉTALLIQUE (MOSFET)

Publication
EP 2856251 A4 20160106 (EN)

Application
EP 13797618 A 20130528

Priority
• US 201213481781 A 20120526
• US 2013042926 W 20130528

Abstract (en)
[origin: WO2013181166A1] A method of fabricating a TFT and IPS with reduced masking operations includes a substrate, a gate, a layer of gate dielectric on the gate and surrounding substrate surface and a semiconducting metal oxide on the gate dielectric. A channel protection layer overlies the gate to define a channel area in the semiconducting metal oxide. A S/D metal layer is patterned on the channel protection layer and a portion of the exposed semiconducting metal oxide to define an IPS area. An organic dielectric material is patterned on the S/D terminals and at an opposed side of the IPS area. The S/D metal is etched to expose the semiconducting metal oxide defining a first IPS electrode. A passivation layer covers the first electrode and a layer of transparent conductive material is patterned on the passivation layer to define a second IPS electrode overlying the first electrode.

IPC 8 full level
G02F 1/1343 (2006.01); **G02F 1/1368** (2006.01); **H01L 29/786** (2006.01)

CPC (source: CN EP)
G02F 1/134363 (2013.01 - CN EP); **G02F 1/13439** (2013.01 - EP); **G02F 1/136227** (2013.01 - CN); **G02F 1/1368** (2013.01 - EP); **H01L 27/1225** (2013.01 - EP); **H01L 27/1288** (2013.01 - EP); **G02F 1/134372** (2021.01 - EP); **G02F 1/136231** (2021.01 - EP); **G02F 1/136236** (2021.01 - EP)

Citation (search report)
• [A] EP 1209748 A1 20020529 - MATSUSHITA ELECTRIC IND CO LTD [JP]
• See references of WO 2013181166A1

Designated contracting state (EPC)
AL AT BE BG CH CY CZ DE DK EE ES FI FR GB GR HR HU IE IS IT LI LT LU LV MC MK MT NL NO PL PT RO RS SE SI SK SM TR

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