

Title (en)

METHOD AND APPARATUS FOR AN ACTIVE NEGATIVE-CAPACITOR CIRCUIT

Title (de)

VERFAHREN UND VORRICHTUNG FÜR EINE AKTIVE NEGATIVVERDICHTERSCHALTUNG

Title (fr)

PROCÉDÉ ET APPAREIL POUR CIRCUIT DE CONDENSATEUR NÉGATIF ACTIF

Publication

**EP 2893637 A1 20150715 (EN)**

Application

**EP 13832732 A 20130902**

Priority

- US 201213602215 A 20120903
- US 201213602216 A 20120903
- US 2013057759 W 20130902

Abstract (en)

[origin: WO2014036542A1] The core concept of this ADC is the high-speed fully-differential comparators which are clocked at 2.64 GHz and used in a 60 GHz transceiver. The comparator consists of a pre-amplifier stage, a capture stage, a regeneration cell and an output latch. The pre-amplifier stage is not clocked; therefore, the pre-amplifier stage does not suffer initialization and transient behavior effects when the clock signal switches state. The transient response of being enabled and disabled is eliminated. Instead, a capture stage transfers the contents of the pre-amplifier stage into a memory regeneration stage. The capture stage is clocked by pulses that are timed to minimize the clock kick-back generated by the memory regeneration stage. The clock kick-back is reduced even when many comparators are coupled to the PGA. The comparators are also aligned right next to each other to minimize the mismatching layout effect.

IPC 8 full level

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CPC (source: CN EP)

**H03M 1/0809** (2013.01 - CN EP); **H03M 1/0818** (2013.01 - CN EP); **H03M 1/124** (2013.01 - EP); **H03M 1/365** (2013.01 - CN EP)

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Designated extension state (EPC)

BA ME

DOCDB simple family (publication)

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