Title (en)

SYSTEM AND METHOD FOR CONTROLLING CENTRAL PROCESSING UNIT POWER WITH GUARANTEED TRANSIENT DEADLINES

Title (de)

SYSTEM UND VERFAHREN ZUR STEUERUNG DER LEISTUNG EINER ZENTRALEN PROZESSOREINHEIT MIT GARANTIERTEN TRANSIENTEN FRISTEN

Title (fr)

SYSTÈME ET PROCÉDÉ DESTINÉS À COMMANDER LA PUISSANCE D'UNE UNITÉ CENTRALE AVEC DES DÉLAIS TRANSITOIRES GARANTIS

Publication

**EP 2915020 A1 20150909 (EN)**

Application

**EP 13776626 A 20130925**

Priority

- US 201213669043 A 20121105
- US 2013061663 W 20130925

Abstract (en)

[origin: WO2014070338A1] Methods, systems and devices that include a dynamic clock and voltage scaling (DCVS) solution configured to compute and enforce performance guarantees to ensure that a processor does not remain in a busy state (e.g., due to transient workloads) for more than a predetermined amount of time above that which is required for that processor to complete its pre-computed steady state workload. The DCVS may adjust the frequency and/or voltage of a processor based on a variable delay to ensure that the processing core only falls behind its steady state workload by, at most, a predefined maximum amount of work, irrespective of the operating frequency or voltage of the processor.

IPC 8 full level

**G06F 1/32** (2006.01)

CPC (source: EP)

**G06F 1/3206** (2013.01); **G06F 1/324** (2013.01); **G06F 1/3296** (2013.01); **G06F 9/4893** (2013.01); Y02D 10/00 (2017.12)

Citation (search report)

See references of WO 2014070338A1

Designated contracting state (EPC)

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BA ME

DOCDB simple family (publication)

**WO 2014070338 A1 20140508**; CN 104756043 A 20150701; CN 104756043 B 20160608; EP 2915020 A1 20150909; JP 2016505913 A 20160225; JP 5930504 B2 20160608; KR 101578336 B1 20151216; KR 20150083883 A 20150720

DOCDB simple family (application)

**US 2013061663 W 20130925**; CN 201380057181 A 20130925; EP 13776626 A 20130925; JP 2015540674 A 20130925; KR 20157014652 A 20130925