Title (en)

PRINTED CIRCUIT BOARD HAVING A LAYER STRUCTURE

Title (de)

LEITERPLATTE IM LAGENAUFBAU

Title (fr)

CARTE DE CIRCUIT IMPRIMÉ À STRUCTURE EN COUCHES

Publication

EP 2948965 A1 20151202 (DE)

Application

EP 14701333 A 20140120

Priority

- DE 102013100622 A 20130122
- EP 2014050997 W 20140120

Abstract (en)

[origin: WO2014114584A1] The invention relates to a printed circuit board having a layer structure, which accommodates a plurality of electric circuits (1, 2). The electric circuits are separated from each other by an insulating barrier layer (61) having a minimum thickness (Di) and a minimum distance (D0) between conducting components of the electric circuits.

IPC 8 full level

H01F 27/28 (2006.01); **H01F 19/08** (2006.01); **H01F 27/32** (2006.01)

CPC (source: EP US)

H01F 5/00 (2013.01 - US); **H01F 27/2804** (2013.01 - EP US); H01F 27/323 (2013.01 - EP US); H01F 2019/085 (2013.01 - EP US); H01F 2027/2809 (2013.01 - EP US); H01F 2027/2819 (2013.01 - EP US)

Citation (search report)

See references of WO 2014114584A1

Citation (examination)

- DE 102007034750 A1 20080306 - AVAGO TECHNOLOGIES GENERAL IP [SG]
- DE 10217580 A1 20031106 - EUPEC GMBH & CO KG [DE]

Designated contracting state (EPC)

AL AT BE BG CH CY CZ DE DK EE ES FI FR GB GR HR HU IE IS IT LI LT LU LV MC MK MT NL NO PL PT RO RS SE SI SK SM TR

Designated extension state (EPC)

BA ME

DOCDB simple family (publication)

DE 102013100622 A1 20140724; **DE 102013100622 B4 20180301**; CN 105009235 A 20151028; EP 2948965 A1 20151202; US 2015357113 A1 20151210; US 9793042 B2 20171017; WO 2014114584 A1 20140731

DOCDB simple family (application)

DE 102013100622 A 20130122; CN 201480005660 A 20140120; EP 14701333 A 20140120; EP 2014050997 W 20140120; US 201414762731 A 20140120