

Title (en)
DYNAMIC OPTIMIZATION OF PIPELINED SOFTWARE

Title (de)
DYNAMISCHE OPTIMIERUNG EINER SOFTWAREPIPELINE

Title (fr)
OPTIMISATION DYNAMIQUE DE LOGICIEL S'EXÉCUTANT EN PIPELINE

Publication
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Application
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Priority
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Abstract (en)
[origin: US2014359591A1] In an embodiment, a system includes a processor including at least one core to execute operations of a loop that includes S stages. The system also includes stage insertion means for adding a delay stage to the loop to increase a lifetime of a corresponding register associated with a first variable of the loop and to delay storage of contents of the register. The system also includes a dynamic random access memory (DRAM). Other embodiments are described and claimed.

IPC 8 full level
G06F 9/38 (2006.01); **G06F 9/45** (2006.01); **G06F 9/46** (2006.01)

CPC (source: EP US)
G06F 8/441 (2013.01 - EP US); **G06F 8/4451** (2013.01 - EP US); **G06F 8/4452** (2013.01 - EP US); **G06F 9/3836** (2013.01 - EP US); **G06F 9/384** (2013.01 - EP US); **G06F 9/3863** (2013.01 - EP US); **G06F 8/443** (2013.01 - US)

Citation (search report)

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- [A] US 2010058034 A1 20100304 - ZAKS AYAL [IL]
- [A] CHUNG-CHI JIM LI ET AL: "COMPILER-BASED MULTIPLE INSTRUCTION RETRY", IEEE TRANSACTIONS ON COMPUTERS, IEEE SERVICE CENTER, LOS ALAMITOS, CA, US, vol. 44, no. 1, 1 January 1995 (1995-01-01), pages 35 - 45, XP000526067, ISSN: 0018-9340, DOI: 10.1109/12.368011
- See references of WO 2014193381A1

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US 2014359591 A1 20141204; US 9170792 B2 20151027; CN 105164637 A 20151216; CN 105164637 B 20171219; EP 2997462 A1 20160323; EP 2997462 A4 20170118; EP 2997462 B1 20200311; JP 2016519375 A 20160630; JP 6117432 B2 20170419; KR 101697038 B1 20170116; KR 20150129327 A 20151119; WO 2014193381 A1 20141204

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