

Title (en)  
PRODUCTION OF SPACERS AT THE EDGES OF A TRANSISTOR GATE

Title (de)  
EINBRINGUNG VON ABSTANDHALTERN AN DEN SEITEN EINES TRANSISTOR-GATES

Title (fr)  
RÉALISATION D'ESPACEURS AU NIVEAU DE FLANCS D'UNE GRILLE DE TRANSISTOR

Publication  
**EP 2999001 B1 20190904 (FR)**

Application  
**EP 15184982 A 20150914**

Priority  
FR 1458759 A 20140917

Abstract (en)  
[origin: US2016079388A1] The production of spacers at flanks of a transistor gate, including a step of forming a dielectric layer covering the gate and a peripheral region of a layer of semiconductor material surrounding the gate, including forming a superficial layer covering the gate and the peripheral region; partially removing the superficial layer configured so as to completely remove the superficial layer at the peripheral region while preserving a residual part of the superficial layer at the flanks; and selective etching of the dielectric layer vis-à-vis the material of the residual part of the superficial layer and vis-à-vis the semiconductor material.

IPC 8 full level  
**H01L 29/78** (2006.01); **H01L 21/336** (2006.01)

CPC (source: EP US)  
**H01L 21/283** (2013.01 - US); **H01L 21/31111** (2013.01 - EP US); **H01L 21/31116** (2013.01 - EP US); **H01L 21/31144** (2013.01 - EP US);  
**H01L 29/42364** (2013.01 - US); **H01L 29/51** (2013.01 - US); **H01L 29/517** (2013.01 - US); **H01L 29/6653** (2013.01 - EP US);  
**H01L 29/6656** (2013.01 - EP US); **H01L 29/66628** (2013.01 - EP US); **H01L 21/02326** (2013.01 - EP US); **H01L 21/0234** (2013.01 - EP US);  
**H01L 29/513** (2013.01 - EP US)

Cited by  
EP3396704A1; FR3065576A1; US10446408B2

Designated contracting state (EPC)  
AL AT BE BG CH CY CZ DE DK EE ES FI FR GB GR HR HU IE IS IT LI LT LU LV MC MK MT NL NO PL PT RO RS SE SI SK SM TR

DOCDB simple family (publication)  
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US 2016079388 A1 20160317; US 9543409 B2 20170110

DOCDB simple family (application)  
**EP 15184982 A 20150914**; FR 1458759 A 20140917; US 201514855834 A 20150916