

Title (en)
ARRAY SUBSTRATE, MANUFACTURING METHOD THEREFOR, AND DISPLAY APPARATUS

Title (de)
ARRAYSUBSTRAT, HERSTELLUNGSVERFAHREN DAFÜR UND ANZEIGEVORRICHTUNG

Title (fr)
SUBSTRAT DE RÉSEAU, SON PROCÉDÉ DE FABRICATION ET APPAREIL D’AFFICHAGE

Publication
EP 3054483 A4 20170510 (EN)

Application
EP 14847683 A 20140709

Priority
• CN 201310462378 A 20130930
• CN 2014081898 W 20140709

Abstract (en)
[origin: US2016013210A1] A method for manufacturing an array substrate which includes: depositing a gate metal film on a base substrate, and forming a first pattern including the gate electrode by a first patterning process; depositing a gate insulating film, a first transparent conductive film, a source/drain metal film and a doped a-Si film sequentially, and forming a second pattern including the pixel electrode, the source electrode, the drain electrode and a doped semiconductor layer by a second patterning process; depositing an a-Si film, and forming a third pattern including a TFT channel, the semiconductor layer and a gate insulating layer via-hole by a third patterning process; depositing a passivation layer film, and forming a fourth pattern including a passivation layer via-hole by a fourth patterning process, the passivation layer via-hole being arranged at a position corresponding to the gate insulating layer via-hole; and depositing a second transparent conductive film on the base substrate with the fourth pattern, and forming a fifth pattern including an electrical connector by a fifth patterning process.

IPC 8 full level
H01L 27/12 (2006.01)

CPC (source: EP US)
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H01L 27/1288 (2013.01 - EP US)

Citation (search report)
• [I] US 2008191211 A1 20080814 - YANO SHINICHI [JP], et al
• [A] US 2011013130 A1 20110120 - CHOI SEUNGJIN [CN], et al
• See references of WO 2015043282A1

Cited by
CN108807421A

Designated contracting state (EPC)
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US 201414422334 A 20140709; CN 201310462378 A 20130930; CN 2014081898 W 20140709; EP 14847683 A 20140709