Title (en)

CLOCK SPURS REDUCTION TECHNIQUE

Title (de)

VERFAHREN ZUR REDUZIERUNG VON TAKTVERSÄTZEN

Title (fr)

TECHNIQUE DE RÉDUCTION DE TRACES D'HORLOGE

Publication

EP 3060930 A1 20160831 (EN)

Application

EP 14815427 A 20141021

Priority

- US 201361894702 P 20131023
- IB 2014002450 W 20141021

Abstract (en)

[origin: WO2015059564A1] Aspects of the disclosure provide a circuit having a jittered clock generator. The jittered clock generator is configured to add jitter of a controlled characteristic to a first clock signal of a clock frequency to generate a second clock signal to be used by a transceiver for operating at a radio frequency. The jitter of the controlled characteristic adjusts a clock harmonic at the radio frequency of the transceiver.

IPC 8 full level

G01R 31/317 (2006.01)

CPC (source: EP)

G01R 31/31709 (2013.01); **H03K 5/156** (2013.01); **H03K 5/1565** (2013.01)

Citation (search report)

See references of WO 2015059564A1

Designated contracting state (EPC)

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Designated extension state (EPC)

BA ME

DOCDB simple family (publication)

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