

Title (en)

HANDLING SLOWER SCAN OUTPUTS AT OPTIMAL FREQUENCY

Title (de)

HANDHABUNG LANGSAMER SCAN-AUSGABEN MIT OPTIMALER FREQUENZ

Title (fr)

GESTION DE SORTIES DE BALAYAGE PLUS LENT À UNE FRÉQUENCE OPTIMALE

Publication

**EP 3090268 B1 20190904 (EN)**

Application

**EP 14875966 A 20141231**

Priority

- US 201314145293 A 20131231
- US 2014073090 W 20141231

Abstract (en)

[origin: US2015185283A1] An embodiment provides a circuit for testing an integrated circuit. The circuit includes a scan compression architecture driven by a scan clock and generates M scan outputs, where M is an integer. A clock divider is configured to divide the scan clock by k to generate k number of phase-shifted scan clocks, where k is an integer. A packing logic is coupled to the scan compression architecture and generates kM slow scan outputs in response to the M scan outputs and the k number of phase shifted scan clocks. The packing logic further includes M number of packing elements and each packing element of the M number of packing elements receives a scan output of the M scan outputs. Each packing element includes k number of flip-flops and each flip-flop of the k number of flip-flops in a packing element receives a scan output of the M scan outputs. Each flip-flop receives a phase-shifted scan clock of the k number of phase-shifted scan clocks, such that each flip-flop generates a slow scan output of the kM slow scan outputs in response to the scan output and the phase-shifted scan clock.

IPC 8 full level

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CPC (source: EP US)

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