Title (en)

WRITE ASSIST SRAM CIRCUITS AND METHODS OF OPERATION

Title (de)

SCHREIBUNTERSTÜTZENDE SRAM-SCHALTUNGEN UND VERFAHREN ZUM BETRIEB

Title (fr)

CIRCUITS SRAM D'ASSISTANCE À L'ÉCRITURE ET PROCÉDÉS DE FONCTIONNEMENT

Publication

EP 3149736 A1 20170405 (EN)

Application

EP 15843819 A 20150925

Priority

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- US 2015052497 W 20150925

Abstract (en)

[origin: CN106062878A] A two-transistor memory cell based upon a thyristor for an SRAM integrated circuit is described together with methods of operation. The memory cell can be implemented in different combinations of MOS and bipolar select transistors, or without select transistors, with thyristors in a semiconductor substrate with shallow trench isolation. Standard CMOS process technology can be used to manufacture the SRAM.

IPC 8 full level

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CPC (source: EP US)

G11C 11/39 (2013.01 - EP US); **G11C 11/418** (2013.01 - EP US); **G11C 11/419** (2013.01 - EP US); **H01L 21/8249** (2013.01 - EP); **H01L 27/0623** (2013.01 - EP); **H10B 10/10** (2023.02 - EP); **H10B 10/12** (2023.02 - EP); G11C 11/4113 (2013.01 - EP US); G11C 11/416 (2013.01 - EP US); H01L 27/0821 (2013.01 - EP); H01L 27/0826 (2013.01 - EP)

Designated contracting state (EPC)

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Designated extension state (EPC)

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DOCDB simple family (publication)

CN 106062878 A 20161026; EP 3149736 A1 20170405; EP 3149736 A4 20180124

DOCDB simple family (application)

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