Title (en)

THREE-STATE INVERTER, D-LATCH AND MASTER-SLAVE BISTABLE COMPRISING TFETS

Title (de)

DREISTUFIGER STROMQUELLEN-UMSCHALTER, VERSCHLUSSKUPPLUNGSHEBEL UND BISTABILE MASTER-SLAVE-SCHALTUNG, DIE TUNNEL-FELDEFFEKT-TRANSISTOREN (TFET) UMFASST

Title (fr)

INVERSEUR A TROIS ETATS, BASCULE D A VERROUILLAGE ET BISTABLE MAITRE-ESCLAVE COMPRENANT DES TFET

Publication

EP 3217547 A1 20170913 (FR)

Application

EP 17160241 A 20170310

Priority

FR 1652056 A 20160311

Abstract (en)

[origin: US10110203B2] Tri-state inverter includes a n-TFET and a p-TFET, the drain of the n-TFET being connected to the drain of the p-TFET and to an output of the tri-state inverter, the gates of the n-TFET and p-TFET being connected to an input of the tri-state inverter, and a control circuit able to apply a first control voltage on the source of the n-TFET and a second control voltage on the source of the p-TFET, the values of the first and second control voltages being positive or zero, wherein, when the tri-state inverter is intended to work as an inverter, the value of the first control voltage is lower than the value of the second control voltage, and when the tri-state inverter is intended to be tri-stated, the value of the first control voltage is higher than the value of the second control voltage.

Abstract (fr)

Inverseur à trois états (108, 112) comprenant : - un premier n-TFET (118, 128) et un premier p-TFET (116, 126), le drain du n-TFET étant connecté au drain du p-TFET et à une sortie de l'inverseur à trois états, les grilles du n-TFET et du p-TFET étant connectées à une entrée de l'inverseur à trois états ; - un circuit de commande apte à appliquer une première tension de commande sur la source du n-TFET et une seconde tension de commande sur la source du p-TFET, les première et seconde tensions de commande étant positives ; et, lorsque l'inverseur à trois états est destiné à fonctionner comme un inverseur, la première tension de commande est inférieure à la seconde tension de commande, et lorsque l'inverseur à trois états est destiné à être dans un état haute impédance, la première tension de commande est supérieure à la seconde tension de commande.

IPC 8 full level

H03K 3/038 (2006.01); **H03K 19/094** (2006.01)

CPC (source: EP US)

H03K 3/012 (2013.01 - US); **H03K 3/038** (2013.01 - EP US); **H03K 3/35625** (2013.01 - US); **H03K 19/0002** (2013.01 - EP US); **H03K 19/09429** (2013.01 - EP US)

Citation (applicant)

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Designated contracting state (EPC)

AL AT BE BG CH CY CZ DE DK EE ES FI FR GB GR HR HU IE IS IT LI LT LU LV MC MK MT NL NO PL PT RO RS SE SI SK SM TR

Designated extension state (EPC)

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