

Title (en)

HIGH GAIN LOAD CIRCUIT FOR A DIFFERENTIAL PAIR USING DEPLETION MODE TRANSISTORS

Title (de)

LASTSCHALTUNG MIT HOHER VERSTÄRKUNG FÜR EIN DIFFERENZPAAR MIT VERARMUNGSMODUS-TRANSISTOREN

Title (fr)

CIRCUIT DE CHARGE À GAIN ÉLEVÉ POUR UNE PAIRE DIFFÉRENTIELLE UTILISANT DES TRANSISTORS À APPAUVRISSEMENT

Publication

EP 3228002 A1 20171011 (EN)

Application

EP 15825667 A 20151204

Priority

- US 201462087987 P 20141205
- US 2015063996 W 20151204

Abstract (en)

[origin: WO2016090248A1] A differential pair gain stage is disclosed. In one embodiment, the gain stage includes a differential pair of depletion-mode transistors, including a first and a second n-type transistor. In certain embodiments of the invention, the depletion mode transistor may be GaN (gallium nitride) field effect transistors. The gain stage includes an active load including one or more depletion mode transistors electrically coupled to at least one of the drains of depletion mode transistors of the differential pair. The active load may include a source follower for maintaining the AC voltages at the drains of the differential pair at a constant value and may further include a casocde stage for setting a fixed drain source voltage across the output transistors to increase the output impedance and gain of the stage.

IPC 8 full level

G05F 3/26 (2006.01); **H03F 3/45** (2006.01)

CPC (source: EP US)

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Citation (search report)

See references of WO 2016090248A1

Citation (examination)

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Designated contracting state (EPC)

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Designated extension state (EPC)

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DOCDB simple family (application)

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