

Title (en)  
 BIOINFORMATICS SYSTEMS, APPARATUSES, AND METHODS EXECUTED ON AN INTEGRATED CIRCUIT PROCESSING PLATFORM

Title (de)  
 BIOINFORMATIKSYSTEME, VORRICHTUNGEN UND AUF EINER VERARBEITUNGSPLATTFORM EINER INTEGRIERTEN SCHALTUNG AUSGEFÜHRTE VERFAHREN

Title (fr)  
 SYSTÈMES BIO-INFORMATIQUES, APPAREILS ET PROCÉDÉS EXÉCUTÉS SUR UNE PLATEFORME DE TRAITEMENT À CIRCUIT INTÉGRÉ

Publication  
**EP 3259590 A4 20181017 (EN)**

Application  
**EP 16753186 A 20160219**

Priority  
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 • US 201562127232 P 20150302  
 • US 2016018765 W 20160219

Abstract (en)  
 [origin: WO2016134310A1] A system, method and apparatus for executing an HMM analysis on genetic sequence data includes an integrated circuit formed of a set of hardwired digital logic circuits that are interconnected by physical electrical interconnects. One of the physical electrical interconnects forms an input to the integrated circuit that may be connected with an electronic data source for receiving reads of genomic data. The hardwired digital logic circuits may be arranged as a set of processing engines, each processing engine being formed of a subset of the hardwired digital logic circuits to perform one or more steps in the HMM analysis on the reads of genomic data. Each subset of the hardwired digital logic circuits may be formed in a wired configuration to perform the one or more steps in the HMM analysis.

IPC 8 full level  
**G16B 50/00** (2019.01); **G16B 30/10** (2019.01); **G16B 50/30** (2019.01)

CPC (source: EP US)  
**G16B 30/00** (2019.01 - EP); **G16B 30/10** (2019.01 - EP US); **G16B 50/00** (2019.01 - EP US); **G16B 50/30** (2019.01 - EP US)

Citation (search report)  
 • [YA] US 2014200166 A1 20140717 - VAN ROOYEN PIETER [US], et al  
 • [YA] US 2014371109 A1 20141218 - MCMILLEN ROBERT J [US], et al  
 • [IY] JUAN FERNANDO EUSSE ET AL: "A Protein Sequence Analysis Hardware Accelerator Based on Divergences", INTERNATIONAL JOURNAL OF RECONFIGURABLE COMPUTING, vol. 2012, 1 January 2012 (2012-01-01), Cairo / New York, pages 1 - 19, XP055503584, ISSN: 1687-7195, DOI: 10.1155/2012/201378  
 • [IY] ARPITH C JACOB ET AL: "Preliminary results in accelerating profile HMM search on FPGAs", PARALLEL AND DISTRIBUTED PROCESSING SYMPOSIUM, 2007. IPDPS 2007. IEEE INTERNATIONAL, IEEE, PI, 20 September 2008 (2008-09-20), pages 1 - 8, XP031175492, ISBN: 978-1-4244-0909-9  
 • [IY] OLIVER T ET AL: "Integrating FPGA acceleration into HMMer", PARALLEL COMPUTING, ELSEVIER, AMSTERDAM, NL, vol. 34, no. 11, 1 November 2008 (2008-11-01), pages 681 - 691, XP025610243, ISSN: 0167-8191, [retrieved on 20080920], DOI: 10.1016/J.PARCO.2008.08.003  
 • See references of WO 2016134310A1

Designated contracting state (EPC)  
 AL AT BE BG CH CY CZ DE DK EE ES FI FR GB GR HR HU IE IS IT LI LT LU LV MC MK MT NL NO PL PT RO RS SE SI SK SM TR

DOCDB simple family (publication)  
**WO 2016134310 A1 20160825**; AU 2016219812 A1 20170831; CA 2976923 A1 20160825; EP 3259590 A1 20171227; EP 3259590 A4 20181017; HK 1248806 A1 20181019

DOCDB simple family (application)  
**US 2016018765 W 20160219**; AU 2016219812 A 20160219; CA 2976923 A 20160219; EP 16753186 A 20160219; HK 18108214 A 20180626