

Title (en)

PARALLELIZED EXECUTION OF INSTRUCTION SEQUENCES BASED ON PREMONITORING

Title (de)

PARALLELISIERTE AUSFÜHRUNG VON BEFEHLSFOLGEN AUF DER GRUNDLAGE VON VORÜBERWACHUNG

Title (fr)

EXÉCUTION EN PARALLÈLE DE SÉQUENCES D'INSTRUCTIONS SUR LA BASE D'UNE PRÉSURVEILLANCE

Publication

**EP 3278212 A1 20180207 (EN)**

Application

**EP 15887388 A 20151209**

Priority

- US 201514673884 A 20150331
- US 201514673889 A 20150331
- IB 2015059469 W 20151209

Abstract (en)

[origin: WO2016156955A1] A method includes, in a processor (20) that processes instructions of program code, processing one or more of the instructions by a first hardware thread. Upon detecting that an instruction defined as a parallelization point has been fetched for the first thread, a second hardware thread is invoked to process at least one of the instructions at least partially in parallel with processing of the instructions by the first hardware thread.

IPC 8 full level

**G06F 9/38** (2018.01)

CPC (source: EP)

**G06F 9/3009** (2013.01); **G06F 9/30185** (2013.01); **G06F 9/3808** (2013.01); **G06F 9/3838** (2013.01); **G06F 9/3842** (2013.01); **G06F 9/3851** (2013.01); **G06F 9/3861** (2013.01)

Designated contracting state (EPC)

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Designated extension state (EPC)

BA ME

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