

Title (en)  
SEMICONDUCTOR PACKAGE STRUCTURE WITH A POLYMER GEL SURROUNDING SOLDERS CONNECTING A CHIP TO A SUBSTRATE AND MANUFACTURING METHOD THEREOF

Title (de)  
HALBLEITERGEHÄUSESTRUKTUR MIT EINEM EINEN CHIP MIT EINEM SUBSTRAT VERBINDENDE LÖTMITTEL UMGEBENDEN POLYMERGEL UND HERSTELLUNGSVERFAHREN DAFÜR

Title (fr)  
STRUCTURE DE BOÎTIER À SEMI-CONDUCTEUR AVEC UN GEL POLYMÉRIQUE ENTOURANT DES SOUDURES RELIANT UNE PUCE AVEC UN SUBSTRAT ET SON PROCÉDÉ DE FABRICATION

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Application  
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Abstract (en)  
A manufacturing method of a package structure (100) such as a semiconductor package structure comprises: providing a substrate (110) such as a flexible printed circuit (FPC) board, wherein the substrate (110) comprises a plurality of solder pads (112); forming a patterned solder resist layer (120) on the substrate (110), wherein the patterned solder resist layer (120) comprises a plurality of stepped openings (122) exposing the solder pads (112) respectively; disposing a polymer gel (130) on a top surface of the patterned solder resist layer (120), wherein the polymer gel (130) at least surrounds a disposing region of the solder pads (112) and is disposed between adjacent two of the solder pads (112); disposing a plurality of solders (140) on the solder pads (112) respectively, wherein the solders (140) are located in the stepped openings (122) respectively; disposing a chip (150) on the substrate (110), wherein the chip (150) comprises an active surface (152) and a plurality of bond pads (154) located on the active surface (152) and the bond pads (154) are connected to the solder pads (112) through the solders (140); and performing a reflow process on the solders (140), such that the solders (140) completely fill the stepped openings (122) of the patterned solder resist layer (120) and the polymer gel (130) is filled between a top surface of the patterned solder resist layer (120) and the active surface (152) and fills between two adjacent solders (140).

IPC 8 full level  
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CPC (source: CN EP US)  
**H01L 21/56** (2013.01 - CN); **H01L 21/563** (2013.01 - EP US); **H01L 23/293** (2013.01 - US); **H01L 23/31** (2013.01 - CN); **H01L 23/49816** (2013.01 - EP US); **H01L 24/03** (2013.01 - US); **H01L 24/09** (2013.01 - US); **H01L 24/16** (2013.01 - EP US); **H01L 24/29** (2013.01 - EP US); **H01L 24/32** (2013.01 - EP US); **H01L 24/73** (2013.01 - EP US); **H01L 24/80** (2013.01 - CN); **H01L 24/92** (2013.01 - EP US); **H01L 23/4985** (2013.01 - EP US); **H01L 23/49894** (2013.01 - EP US); **H01L 23/564** (2013.01 - EP US); **H01L 24/11** (2013.01 - EP US); **H01L 24/13** (2013.01 - EP US); **H01L 24/27** (2013.01 - EP US); **H01L 24/81** (2013.01 - EP US); **H01L 24/83** (2013.01 - EP US); **H01L 2224/03622** (2013.01 - US); **H01L 2224/03849** (2013.01 - US); **H01L 2224/0401** (2013.01 - EP US); **H01L 2224/04026** (2013.01 - EP US); **H01L 2224/05568** (2013.01 - EP US); **H01L 2224/05571** (2013.01 - EP US); **H01L 2224/056** (2013.01 - EP US); **H01L 2224/0569** (2013.01 - EP US); **H01L 2224/0903** (2013.01 - US); **H01L 2224/1132** (2013.01 - EP US); **H01L 2224/13007** (2013.01 - EP US); **H01L 2224/13013** (2013.01 - EP US); **H01L 2224/13021** (2013.01 - EP US); **H01L 2224/16012** (2013.01 - EP US); **H01L 2224/16112** (2013.01 - EP US); **H01L 2224/16227** (2013.01 - EP US); **H01L 2224/2732** (2013.01 - EP US); **H01L 2224/27848** (2013.01 - EP US); **H01L 2224/29011** (2013.01 - EP US); **H01L 2224/29013** (2013.01 - EP US); **H01L 2224/2919** (2013.01 - EP US); **H01L 2224/32225** (2013.01 - EP US); **H01L 2224/73103** (2013.01 - EP US); **H01L 2224/73204** (2013.01 - EP US); **H01L 2224/81192** (2013.01 - EP US); **H01L 2224/81815** (2013.01 - EP US); **H01L 2224/83192** (2013.01 - EP US); **H01L 2224/83856** (2013.01 - EP US); **H01L 2224/9211** (2013.01 - EP US)

Citation (search report)  
• [IY] WO 2010084858 A1 20100729 - PANASONIC ELEC WORKS CO LTD [JP], et al  
• [Y] WO 2005024939 A1 20050317 - GEN ELECTRIC [US], et al  
• [Y] US 2010123256 A1 20100520 - YODA TSUYOSHI [JP], et al  
• [A] US 2012306095 A1 20121206 - HAN KYUJIN [KR]  
• [A] EP 1482547 A2 20041201 - XEROX CORP [US]  
• [A] JP H07254632 A 19951003 - CLARION CO LTD  
• [A] US 2012039056 A1 20120216 - OPPERMAN HANS-HERMANN [DE], et al  
• [A] EP 1306897 A2 20030502 - FUJITSU LTD [JP]  
• [A] US 2002064930 A1 20020530 - ISHIKAWA NATSUYA [JP]  
• [A] JP H10335527 A 19981218 - NEC CORP  
• [A] JP 2007128982 A 20070524 - NEC CORP  
• [A] US 2013307144 A1 20131121 - YU CHEN-HUA [TW], et al  
• [A] US 2008023829 A1 20080131 - KOK CHI WAH [CN], et al

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