

Title (en)

METHOD FOR INTEGRATING AT LEAST ONE 3D INTERCONNECTION FOR THE MANUFACTURE OF AN INTEGRATED CIRCUIT

Title (de)

VERFAHREN ZUR INTEGRATION VON MINDESTENS EINER 3D-VERBINDUNG ZUR HERSTELLUNG EINER INTEGRIERTEN SCHALTUNG

Title (fr)

PROCEDE D'INTEGRATION D'AU MOINS UNE INTERCONNEXION 3D POUR LA FABRICATION DE CIRCUIT INTEGRE

Publication

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Application

EP 16770715 A 20160914

Priority

- FR 1558544 A 20150914
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Abstract (en)

[origin: WO2017046153A1] The invention relates to a method for integrating at least one interconnection for the manufacture of an integrated circuit, including a step of depositing at least one insulating body (7) onto a substrate (1) including a horizontal surface (1a), said insulating body (7) comprising a first wall (7b) extending from the horizontal surface (1a) of the substrate (1) to a high point of said insulating body (7), and a step of depositing a one-piece electrical structure (9) which is made of an electrically conductive material and extends on the horizontal surface (1a) of the substrate (1) and the first wall (7b) of the insulating body (7), the first wall (7b) being vertically angled by more than 10 µm and having a rising slope extending from the horizontal surface (1a) of the substrate (1) to the high point of said insulating body (7).

IPC 8 full level

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CPC (source: EP US)

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Citation (search report)

See references of WO 2017046153A1

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