Title (en)

THROUGH-MEMORY-LEVEL VIA STRUCTURES BETWEEN STAIRCASE REGIONS IN A THREE-DIMENSIONAL MEMORY DEVICE AND METHOD OF MAKING THEREOF

Title (de)

KONTAKTLOCHSTRUKTUREN DURCH SPEICHEREBENE ZWISCHEN STAIRCASE-REGIONEN IN EINER DREIDIMENSIONALEN SPEICHERVORRICHTUNG UND VERFAHREN ZUR HERSTELLUNG DAVON

Title (fr)

STRUCTURES DE TROUS D'INTERCONNEXION TRAVERSANT DES NIVEAUX DE MÉMOIRE ENTRE DES RÉGIONS EN CAGE D'ESCALIER DANS UN DISPOSITIF TRIDIMENSIONNEL DE MÉMOIRE ET PROCÉDÉ POUR LEUR FABRICATION

Publication

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Application

EP 17708646 A 20170221

Priority

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- US 2017018714 W 20170221

Abstract (en)

[origin: US2017352678A1] Lower level metal interconnect structures are formed over a substrate with semiconductor devices thereupon. A semiconductor material layer and an alternating stack of spacer dielectric layers and insulating layers is formed over the lower level metal interconnect structures. An array of memory stack structures is formed through the alternating stack. Trenches are formed through the alternating stack such that a staircase region is located farther away from a threshold lateral distance from the trenches, while neighboring staircase regions are formed within the threshold lateral distance from the trenches. Portions of the spacer dielectric layers proximal to the trenches are replaced with electrically conductive layers, while a remaining portion of the alternating stack is present in the staircase region. At least one through-memory-level via structure can be formed through the remaining portions of the spacer dielectric layers and the insulating layers to provide a vertically conductive path through a memory-level assembly.

IPC 8 full level

H10B 43/23 (2023.01); **H01L 29/66** (2006.01); **H01L 29/792** (2006.01); **H10B 43/27** (2023.01); **H10B 43/35** (2023.01); **H10B 43/40** (2023.01); **H10B 43/50** (2023.01)

CPC (source: EP US)

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