

Title (en)

REDUCED SIZE SPLIT GATE NON-VOLATILE FLASH MEMORY CELL AND METHOD OF MAKING SAME

Title (de)

VERKLEINERTE NICHTFLÜCHTIGE SPLIT-GATE-FLASH-SPEICHERZELLE UND VERFAHREN ZUR HERSTELLUNG DAVON

Title (fr)

CELLULE DE MÉMOIRE FLASH NON VOLATILE À GRILLE DIVISÉE DE TAILLE RÉDUITE, ET SON PROCÉDÉ DE FABRICATION

Publication

EP 3449501 B1 20210127 (EN)

Application

EP 17779530 A 20170327

Priority

- CN 201610216805 A 20160408
- US 201715468541 A 20170324
- US 2017024310 W 20170327

Abstract (en)

[origin: US2017330949A1] A reduced size non-volatile memory cell array is achieved by forming first trenches in an insulation layer in the row direction, filling the first trenches with insulation material, forming second trenches in the insulation layer in the column direction, forming the STI isolation material in the second trenches, and forming the source regions through the first trenches. Alternately, the STI isolation regions can be made continuous, and the source diffusion implant has sufficient energy to form continuous source line diffusions that each extend across the active regions and under the STI isolation regions. This allows control gates of adjacent memory cell pairs to be formed closer together.

IPC 8 full level

H01L 21/70 (2006.01); **H01L 27/11524** (2017.01); **H01L 29/423** (2006.01); **H01L 29/66** (2006.01); **H01L 29/788** (2006.01)

CPC (source: CN EP KR US)

H01L 21/70 (2013.01 - EP US); **H01L 29/40114** (2019.07 - EP US); **H01L 29/42328** (2013.01 - EP KR US); **H01L 29/66825** (2013.01 - EP KR US); **H01L 29/7881** (2013.01 - EP KR US); **H10B 41/00** (2023.02 - CN); **H10B 41/20** (2023.02 - KR); **H10B 41/30** (2023.02 - EP US); **H10B 41/35** (2023.02 - EP KR US)

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DOCDB simple family (publication)

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