

Title (en)  
SYNCHRONIZABLE RING OSCILLATORS

Title (de)  
SYNCHRONISIERBARE RINGOSZILLATOREN

Title (fr)  
OSCILLATEURS EN ANNEAU SYNCHRONISABLES

Publication  
**EP 3503391 A1 20190626 (EN)**

Application  
**EP 18212558 A 20181214**

Priority  
US 201715853171 A 20171222

Abstract (en)  
Several ring oscillator constructions are provided. The ring oscillator includes a plurality of logic gates connected in a ring configuration. An output of each except a last of the plurality of logic gates is used as an input for a next one of the plurality of logic gates. The output of the last of the plurality of logic gates is fed back to and used as an input for a first of the plurality of logic gates. A logic gate of the plurality of logic gates includes an enable input to receive an enable signal to enable the logic gate and thereby the ring oscillator. The plurality of logic gates includes at least one controlled logic gate that also includes a clock input to receive a clock signal to control the at least one controlled logic gate and thereby synchronize the ring oscillator to the clock signal.

IPC 8 full level  
**H03K 3/03** (2006.01)

CPC (source: CN EP US)  
**H03K 3/0315** (2013.01 - EP US); **H03K 3/0322** (2013.01 - CN); **H03K 5/159** (2013.01 - US); **H03L 7/24** (2013.01 - US); **H03K 19/20** (2013.01 - US)

Citation (search report)  
• [A] JP 2008003047 A 20080110 - RENESAS TECH CORP  
• [XI] GIERKINK S L J: "A 2.5 Gb/s Run-Length-Tolerant Burst-Mode CDR Based on a 1/8th-Rate Dual Pulse Ring Oscillator", IEEE JOURNAL OF SOLID-STATE CIRCUITS, IEEE SERVICE CENTER, PISCATAWAY, NJ, USA, vol. 43, no. 8, 1 August 2008 (2008-08-01), pages 1763 - 1771, XP011231775, ISSN: 0018-9200, DOI: 10.1109/JSSC.2008.926736  
• [X] DOLEV DANNY ET AL: "Rigorously modeling self-stabilizing fault-tolerant circuits: An ultra-robust clocking scheme for systems-on-chip", JOURNAL OF COMPUTER AND SYSTEM SCIENCES, ACADEMIC PRESS, INC., LONDON, GB, vol. 80, no. 4, 15 January 2014 (2014-01-15), pages 860 - 900, XP028615010, ISSN: 0022-0000, DOI: 10.1016/J.JCSS.2014.01.001

Citation (examination)  
• US 2017155395 A1 20170601 - GROLLITSCH WERNER [AT], et al  
• US 2017117907 A1 20170427 - GROLLITSCH WERNER [AT]  
• US 2009243734 A1 20091001 - MARGITTAI GAVRIL [US]

Designated contracting state (EPC)  
AL AT BE BG CH CY CZ DE DK EE ES FI FR GB GR HR HU IE IS IT LI LT LU LV MC MK MT NL NO PL PT RO RS SE SI SK SM TR

Designated extension state (EPC)  
BA ME

DOCDB simple family (publication)  
**EP 3503391 A1 20190626**; CN 110011643 A 20190712; CN 110011643 B 20230808; JP 2019154023 A 20190912; JP 7450332 B2 20240315; US 10469060 B1 20191105

DOCDB simple family (application)  
**EP 18212558 A 20181214**; CN 201811561036 A 20181220; JP 2018238584 A 20181220; US 201715853171 A 20171222