

Title (en)
3D SEMICONDUCTOR DEVICE AND STRUCTURE

Title (de)
3D-HALBLEITERBAUELEMENT UND STRUKTUR DAMIT

Title (fr)
DISPOSITIF TRIDIMENSIONNEL À SEMI-CONDUCTEUR ET STRUCTURE

Publication
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Application
EP 17859869 A 20170919

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- US 201662432575 P 20161211
- US 201662440720 P 20161230
- US 201762457838 P 20170211
- US 201762460989 P 20170220
- US 201762471963 P 20170316
- US 201762480529 P 20170402
- US 201762484398 P 20170412
- US 201762488821 P 20170423
- US 201762517152 P 20170608
- US 201762530173 P 20170708
- US 201762535265 P 20170721
- US 201762549952 P 20170824
- US 2017052359 W 20170919

Abstract (en)
[origin: WO2018071143A2] A 3D device, the device comprising: a first stratum comprising a first bit-cell array, the first bit-cell array includes three independent first rows; a second stratum including a second bit-cell array, the second bitcell array includes three independent second rows, where the second stratum overlays the first stratum; and at least three vertical bitlines each connected to respective three horizontal first bitlines and three horizontal second bitlines, where the three horizontal first bitlines include control of the first bit-cell array, where the three horizontal second bitlines include control of the second bit-cell array, and where each of the three vertical bitlines could be used to control a different one of the three independent first rows, or control a different one of the three independent second rows

IPC 8 full level
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CPC (source: EP)
H01L 27/0688 (2013.01); **H10B 10/12** (2023.02); **H10B 41/20** (2023.02)

Citation (search report)

- [I] US 2012182801 A1 20120719 - LUE HANG-TING [TW]
- [XI] US 2015340366 A1 20151126 - LIM JOON-SUNG [KR], et al

Designated contracting state (EPC)
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