

Title (en)

PARALLELISABLE METHOD FOR INTEGRATING POWER CHIPS AND POWER ELECTRONICS MODULES

Title (de)

PARALLELISIERBARES VERFAHREN ZUR INTEGRATION VON LEISTUNGSCHEIPS UND LEISTUNGSELEKTRONIKMODULEN

Title (fr)

PROCEDE D'INTEGRATION DE PUCES DE PUISSANCE PARALLELISABLE ET MODULES ELECTRONIQUES DE PUISSANCE

Publication

EP 3552235 A1 20191016 (FR)

Application

EP 17822726 A 20171205

Priority

- FR 1662335 A 20161212
- FR 2017053392 W 20171205

Abstract (en)

[origin: WO2018109315A1] The method comprises the steps of 1) producing first and second blanks (EB1) including reserved-space defining means (HM1, HM2), by laminating insulating and conductive inner layers (PP, CP) on copper plates forming a base (MB1), at least one electronic chip being sandwiched between the blanks, said blanks being produced such that their upper lamination surfaces have matching profiles, 2) stacking and fitting the blanks via their matching profiles, and 3) press-fitting the blanks to form a laminated sub-assembly for an integrated power electronics device. The method uses IMS-type techniques.

IPC 8 full level

H01L 25/11 (2006.01); **H01L 23/473** (2006.01); **H01L 23/538** (2006.01); **H05K 1/14** (2006.01); **H05K 3/36** (2006.01)

CPC (source: EP US)

H01L 23/3114 (2013.01 - US); **H01L 23/473** (2013.01 - EP); **H01L 23/49838** (2013.01 - US); **H01L 23/5385** (2013.01 - EP US);
H01L 23/5389 (2013.01 - US); **H01L 25/117** (2013.01 - EP US); **H01L 25/18** (2013.01 - US); **H03K 17/60** (2013.01 - US);
H01L 25/18 (2013.01 - EP); **H05K 1/056** (2013.01 - EP); **H05K 2201/10166** (2013.01 - EP)

Citation (search report)

See references of WO 2018109315A1

Designated contracting state (EPC)

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Designated extension state (EPC)

BA ME

DOCDB simple family (publication)

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JP 2020501381 A 20200116; US 10734368 B2 20200804; US 2020185365 A1 20200611; WO 2018109315 A1 20180621

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FR 1662335 A 20161212; CN 201780086323 A 20171205; EP 17822726 A 20171205; FR 2017053392 W 20171205;
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