Title (en)
REDUNDANT PROCESSOR ARCHITECTURE

Title (de)
REDUNDANTE PROZESSORARCHITEKTUR

Title (fr)
ARCHITECTURE REDONDANTE DE PROCESSEUR

Publication
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Application
EP 17825518 A 20171221

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Abstract (en)
[origin: WO2018134023A1] The invention relates to an assembly (101) with a first processor (103) and a second processor (103); wherein the first processor (103) has a first core (107), a second core (109), and a control entity (113); the second processor (105) has a first core (115); and the first core (107) and the second core (109) of the first processor (103) and the first core (115) of the second processor (105) are designed to carry out a first procedure. The control entity (113) of the first processor (103) is designed to carry out the following steps: comparing the result of carrying out the first procedure on the first core (107) of the first processor (103) with the result of carrying out the first procedure on the second core (109) of the first processor (103); and comparing the result of carrying out the first procedure on the first core (107) of the first processor (103) and the result of carrying out the first procedure on the second core (109) of the first processor (103) with the result of carrying out the first procedure on the first core (115) of the second processor (105) if the results of carrying out the first procedure on the first core (107) and the second core (109) of the first processor (103) deviate from each other.

IPC 8 full level
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Citation (search report)
See references of WO 2018134023A1

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