

Title (en)
HACKING-RESISTANT COMPUTER DESIGN

Title (de)
HACKING-BESTÄNDIGES COMPUTERDESIGN

Title (fr)
CONCEPTION PAR ORDINATEUR RÉSISTANT AU PIRATAGE

Publication
EP 3583538 A4 20201104 (EN)

Application
EP 17896907 A 20170220

Priority
US 2017018578 W 20170220

Abstract (en)
[origin: WO2018151735A1] A computer architecture is disclosed for implementing a hacking-resistant computing device. The computing device, which could be a mainframe computer, personal computer, smartphone, or any other computing device suitable for network communication, comprises a first partition and a second partition. The second partition can communicate over a network such as the Internet. In contrast, the first partition cannot connect to the Internet, and can directly communicate only with the second partition or with input/output devices directly connected to the first partition. Further, the first partition segments its memory addressing for program code and hardware-protects it from alteration. The second partition is hardware- limited from reading or writing to the memory addressing of the first partition. As a result, the critical data files and program code stored on the first partition are protected from malicious code affecting the second partition.

IPC 8 full level
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G06F 21/78 (2013.01); **G06F 21/85** (2013.01)

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G06F 21/76 (2013.01); **G06F 21/85** (2013.01)

Citation (search report)
• [XI] US 2016308677 A1 20161020 - THOM STEFAN [US], et al
• [XAI] US 2016055102 A1 20160225 - DE CESARE JOSHUA P [US], et al
• [A] US 2014331307 A1 20141106 - ELLIS FRAMPTON E [US]
• See references of WO 2018151735A1

Designated contracting state (EPC)
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WO 2018151735 A1 20180823; CN 110337651 A 20191015; EP 3583538 A1 20191225; EP 3583538 A4 20201104; JP 2020508499 A 20200319;
JP 7027664 B2 20220302; SG 11201706338W A 20180927

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SG 11201706338W A 20170220