Title (en)
GENERAL-PURPOSE PARALLEL COMPUTING ARCHITECTURE

Title (de)
PARALLELE MEHRZWECKRECHNERARCHITEKTUR

Title (fr)
ARCHITECTURE INFORMATIQUE PARALLÈLE POLYVALENTE

Publication
EP 3607454 A1 20200212 (EN)

Application
EP 18780648 A 20180404

Priority
• US 201715481201 A 20170406
• US 2018026108 W 20180404

Abstract (en)
[origin: WO2018187487A1] An apparatus includes multiple parallel computing cores (102), where each computing core is configured to perform one or more processing operations and generate input data. The apparatus also includes multiple parallel coprocessors (112) associated with each computing core. Each computing core is configured to provide the input data generated by that computing core to a designated one of the coprocessors associated with each of the computing cores. The coprocessors are configured to process the input data and generate output data. The apparatus further includes multiple reducer circuits (115). Each computing core is associated with one of the reducer circuits. Each reducer circuit is configured to receive the output data from each of the coprocessors of the associated computing core, to apply one or more functions to the output data, and to provide one or more results to the associated computing core. The computing cores, the coprocessors, and the reducer circuits are arranged laterally side-by-side in a two-dimensional layout.

IPC 8 full level
G06F 15/80 (2006.01)

CPC (source: EP)
G06F 9/5072 (2013.01); **G06F 15/8023** (2013.01); **G06N 3/044** (2023.01); **G06N 3/047** (2023.01); **G06N 3/063** (2013.01); **G06N 3/084** (2013.01); **G06N 3/088** (2013.01); **G06N 7/01** (2023.01); **G06N 20/00** (2018.12); G06N 3/082 (2013.01)

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