

Title (en)
SCHOTTKY-CMOS ASYNCHRONOUS LOGIC CELLS

Title (de)
ASYNCHRONE SCHOTTKY-CMOS-LOGIKZELLEN

Title (fr)
CELLULES LOGIQUES ASYNCHRONES À CMOS SCHOTTKY

Publication
EP 3610573 A4 20210421 (EN)

Application
EP 18783874 A 20180410

Priority
• US 201715484040 A 20170410
• US 2018026817 W 20180410

Abstract (en)
[origin: WO2018191217A1] Integrated circuits described herein implement an x-input logic gate. The integrated circuit includes a plurality of Schottky diodes that includes x Schottky diodes and a plurality of source-follower transistors that includes x source-follower transistors. Each respective source-follower transistor of the plurality of source-follower transistors includes a respective gate node that is coupled to a respective Schottky diode. A first source-follower transistor of the plurality of source-follower transistors is connected serially to a second source-follower transistor of the plurality of source-follower transistors.

IPC 8 full level
H03K 19/017 (2006.01); **H03K 19/0948** (2006.01); **H03K 19/0956** (2006.01); **H03K 19/177** (2020.01)

CPC (source: CN EP)
H03K 19/017 (2013.01 - CN EP); **H03K 19/0948** (2013.01 - CN EP); **H03K 19/0956** (2013.01 - CN EP); **H03K 19/177** (2013.01 - CN EP)

Citation (search report)
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• [XI] US 2006044018 A1 20060302 - CHANG AUGUSTINE W [US]
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• See references of WO 2018191217A1

Designated contracting state (EPC)
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WO 2018191217 A1 20181018; WO 2018191217 A4 20181129; CN 110622419 A 20191227; CN 110622419 B 20210511;
CN 113452362 A 20210928; CN 113452362 B 20220708; EP 3610573 A1 20200219; EP 3610573 A4 20210421; TW 201904198 A 20190116;
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