Title (en)

SIGNAL TRANSMISSION METHOD, TRANSMISSION UNIT, RECEIVING UNIT, AND DISPLAY DEVICE

Title (de)

SIGNALSENDEVERFAHREN, SENDEEINHEIT, EMPFANGSEINHEIT UND ANZEIGEVORRICHTUNG

Title (fr)

PROCÉDÉ DE TRANSMISSION DE SIGNAUX, UNITÉ DE TRANSMISSION, UNITÉ DE RÉCEPTION, ET DISPOSITIF D'AFFICHAGE

Publication

EP 3637407 A4 20210120 (EN)

Application

EP 18812852 A 20180604

Priority

- CN 201710434370 A 20170609
- CN 2018089740 W 20180604

Abstract (en)

[origin: EP3637407A1] The present disclosure relates to a method and device for transmitting a signal in a display device. The display device comprises a timing controller and a source driver. The method is applied to any of a plurality of transmitting units of the timing controller. The plurality of transmitting units correspond to a plurality of receiving units of the source driver in a one-to-one relationship. The method comprises: obtaining a scrambled signal by scrambling, via a scrambler of the transmitting unit, a non-identification signal in a signal to be transmitted, the scrambled signal comprising an identification signal and a scrambled non-identification signal; and transmitting the scrambled signal to a corresponding receiving unit. A signal obtained by scrambling a signal X via the scrambler is X¹⁶+X⁵+X⁴+X³+1, X²⁴+X⁴+X³+X+1 or X³²+X⁷+X⁵+X³+X²+X+1. The present disclosure reduces distortion of an image displayed on a display panel.

IPC 8 full level

G09G 3/20 (2006.01); **G09G 3/36** (2006.01); **G09G 5/00** (2006.01); **H04L 9/12** (2006.01); **H04L 25/03** (2006.01)

CPC (source: CN EP US)

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Citation (search report)

- [I] US 2014192097 A1 20140710 - BAEK DONG-HOON [KR], et al
- [I] US 2012146965 A1 20120614 - BAEK DONG-HOON [KR], et al
- [A] US 2014269954 A1 20140918 - WHITBY-STREVENS COLIN [US]
- [A] US 2006093147 A1 20060504 - KWON WON O [KR], et al
- [A] AMIT KUMAR PANDA ET AL: "FPGA Implementation of 8, 16 and 32 Bit LFSR with Maximum Length Feedback Polynomial Using VHDL", COMMUNICATION SYSTEMS AND NETWORK TECHNOLOGIES (CSNT), 2012 INTERNATIONAL CONFERENCE ON, IEEE, 11 May 2012 (2012-05-11), pages 769 - 773, XP032183105, ISBN: 978-1-4673-1538-8, DOI: 10.1109/CSNT.2012.168
- See references of WO 2018223913A1

Designated contracting state (EPC)

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DOCDB simple family (publication)

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