

Title (en)
FINER GRAIN DYNAMIC RANDOM ACCESS MEMORY

Title (de)
FEINERKÖRNIGER DYNAMISCHER DIREKTZUGRIFFSSPEICHER

Title (fr)
MÉMOIRE VIVE DYNAMIQUE À GRAIN PLU FIN

Publication
EP 3639265 A4 20210106 (EN)

Application
EP 18818644 A 20180518

Priority
• US 201762518575 P 20170612
• US 201815976580 A 20180510
• US 2018033317 W 20180518

Abstract (en)
[origin: WO2018231423A1] Systems, apparatuses, and methods related to dynamic random access memory (DRAM), such as finer grain DRAM, are described. For example, an array of memory cells in a memory device may be partitioned into regions. Each region may include a plurality of banks of memory cells. Each region may be associated with a data channel configured to communicate with a host device. In some examples, each channel of the array may include two or more data pins. The ratio of data pins per channel may be two or four in various examples. Other examples may include eight data pins per channel.

IPC 8 full level
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CPC (source: EP KR)
G11C 5/025 (2013.01 - EP); **G11C 5/04** (2013.01 - EP); **G11C 5/06** (2013.01 - KR); **G11C 5/063** (2013.01 - EP); **G11C 8/12** (2013.01 - EP KR); **G11C 11/408** (2013.01 - EP); **G11C 11/4096** (2013.01 - EP KR)

Citation (search report)
• [XY] US 2009103345 A1 20090423 - MCLAREN MORAY [GB], et al
• [XYI] US 2015270250 A1 20150924 - TAKAMITSU ONDA [JP]
• [Y] US 2010121994 A1 20100513 - KIM KYU-HYOUN [US], et al
• See references of WO 2018231423A1

Designated contracting state (EPC)
AL AT BE BG CH CY CZ DE DK EE ES FI FR GB GR HR HU IE IS IT LI LT LU LV MC MK MT NL NO PL PT RO RS SE SI SK SM TR

DOCDB simple family (publication)
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DOCDB simple family (application)
US 2018033317 W 20180518; CN 201880045249 A 20180518; EP 18818644 A 20180518; KR 20207000849 A 20180518; KR 20217028680 A 20180518