

Title (en)

COMPUTER IMPLEMENTED SYSTEM AND METHOD OF TRANSLATION OF VERIFICATION COMMANDS OF AN ELECTRONIC DESIGN

Title (de)

COMPUTERIMPLEMENTIERTES SYSTEM UND VERFAHREN ZUR ÜBERSETZUNG VON VERIFIZIERUNGSBEFEHLEN EINES ELEKTRONISCHEN DESIGNS

Title (fr)

SYSTÈME ET PROCÉDÉ INFORMATISÉS DE TRADUCTION D'INSTRUCTIONS DE VÉRIFICATION D'UNE CONCEPTION ÉLECTRONIQUE

Publication

EP 3655963 A1 20200527 (EN)

Application

EP 18836208 A 20180719

Priority

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- US 2018042793 W 20180719

Abstract (en)

[origin: WO2019018589A1] A computer implemented method of translation of verification commands of an electronic design, comprises the steps of receiving the electronic design, receiving at least one analog test harness model having at least one indirect branch contribution statement and having at least one of at least one stimulus parameter stored in at least one specification database and at least one measurement parameter stored in at least one specification database and at least one specification parameter stored in at least one specification database, translating the at least one indirect branch contribution statement into a plurality of direct branch contribution operators based at least in part upon the at least one analog test harness model and at least one of at least one stimulus parameter stored in at least one specification database and at least one measurement parameter stored in at least one specification database and at least one specification parameter stored in at least one specification database and generating a netlist based at least in part upon the translation.

IPC 8 full level

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CPC (source: EP)

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