

Title (en)
ANALOG-TO-DIGITAL CONVERTER SYSTEM, ELECTRONIC DEVICE AND ANALOG-TO-DIGITAL CONVERSION METHOD

Title (de)
ANALOG-DIGITAL-WANDLERSYSTEM, ELEKTRONISCHE VORRICHTUNG UND VERFAHREN ZUR ANALOG-DIGITAL-WANDLUNG

Title (fr)
SYSTÈME DE CONVERTISSEUR ANALOGIQUE/NUMÉRIQUE, DISPOSITIF ÉLECTRONIQUE ET PROCÉDÉ DE CONVERSION ANALOGIQUE-NUMÉRIQUE

Publication
EP 3700092 A1 20200826 (EN)

Application
EP 19159150 A 20190225

Priority
EP 19159150 A 20190225

Abstract (en)
An ADC system comprises a coarse ADC for determining a coarse word (CW) representing an input signal, and an incremental ADC (IADC) for determining a fine word (FW) based on a combination of the input signal and a feedback signal. A first combiner (CMB1) generates a first intermediate output word (IW1) by joining the coarse word (CW) and the fine word (FW). A feedback path generates the feedback signal based on the first intermediate output word (IW1). A decimation filter (DEC) generates a second intermediate output word (IW2) by filtering the first intermediate output word (IW1). A correction block (FCAL) determines a correction word (CALW) based on the coarse word (CW), on the first and the second predetermined number of bits and conversion parameters of the incremental ADC. A second combiner generates an output word (OW) by addition of the second intermediate output word (IW2) and the correction word (CALW).

IPC 8 full level
H03M 1/08 (2006.01); **H03M 1/10** (2006.01); **H03M 1/14** (2006.01); **H03M 3/00** (2006.01)

CPC (source: EP US)
H03M 1/1019 (2013.01 - US); **H03M 1/1038** (2013.01 - EP); **H03M 1/14** (2013.01 - EP US); **H03M 3/46** (2013.01 - EP)

Citation (search report)

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- [A] EP 3104530 A1 20161214 - ANALOG DEVICES INC [US]
- [A] EP 2930849 A1 20151014 - ANALOG DEVICES GLOBAL [BM]
- [I] YOUNGCHEOL CHAE ET AL: "A 6.3 W 20 bit Incremental Zoom-ADC with 6 ppm INL and 1 V Offset", IEEE JOURNAL OF SOLID-STATE CIRCUITS., vol. 48, no. 12, 1 December 2013 (2013-12-01), PISCATAWAY, NJ, USA, pages 3019 - 3027, XP055410108, ISSN: 0018-9200, DOI: 10.1109/JSSC.2013.2278737
- [A] MARKUS J ET AL: "Theory and Applications of Incremental $\Delta\Sigma$ Converters", IEEE TRANSACTIONS ON CIRCUITS AND SYSTEMS PART I: REGULAR PAPERS, IEEE SERVICE CENTER, NEW YORK, NY, US, vol. 51, no. 4, 1 April 2004 (2004-04-01), pages 678 - 690, XP011110984, ISSN: 1057-7122, DOI: 10.1109/TCSI.2004.826202

Designated contracting state (EPC)
AL AT BE BG CH CY CZ DE DK EE ES FI FR GB GR HR HU IE IS IT LI LT LU LV MC MK MT NL NO PL PT RO RS SE SI SK SM TR

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BA ME

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EP 3700092 A1 20200826; **EP 3700092 B1 20230830**; CN 114008926 A 20220201; US 11711093 B2 20230725; US 2023138427 A1 20230504; WO 2020173656 A1 20200903

DOCDB simple family (application)
EP 19159150 A 20190225; CN 202080012334 A 20200130; EP 2020052299 W 20200130; US 202017432270 A 20200130