Title (en)

INTEGRATED CIRCUIT MARGIN MEASUREMENT AND FAILURE PREDICTION DEVICE

Title (de)

INTEGRIERTE SCHALTUNGSMARGENMESS- UND AUSFALLVORHERSAGEVORRICHTUNG

Title (fr)

DISPOSITIF DE MESURE DE MARGE DE CIRCUIT INTÉGRÉ ET DE PRÉDICTION DE DÉFAILLANCE

Publication

EP 3710844 B1 20240207 (EN)

Application

EP 18877539 A 20181115

Priority

- US 201762586423 P 20171115
- IL 2018051234 W 20181115

Abstract (en)

[origin: WO2019097516A1] A semiconductor integrated circuit (IC) comprising a signal path combiner, comprising a plurality of input paths and an output path. The IC comprises a delay circuit having an input electrically connected to the output path, the delay circuit delaying an input signal by a variable delay time to output a delayed signal path. The IC may comprise a first storage circuit electrically connected to the output path and a second storage circuit electrically connected to the delayed signal path. The IC comprises a comparison circuit that compares outputs of the signal path combiner and the delayed signal, wherein the comparison circuit comprises a comparison output provided in a comparison data signal to at least one mitigation circuit.

IPC 8 full level

G01R 31/3193 (2006.01); **G01R 31/28** (2006.01); **G01R 31/30** (2006.01)

CPC (source: CN EP IL KR US)

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DOCDB simple family (publication)

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IL 2018051234 W 20181115; CN 201880085236 A 20181115; CN 202310252063 A 20181115; EP 18877539 A 20181115; EP 23220748 A 20181115; ES 18877539 T 20181115; IL 27468820 A 20200514; IL 30608023 A 20230919; JP 2020545016 A 20181115; JP 2022133215 A 20220824; KR 20207016661 A 20181115; KR 20237002918 A 20181115; TW 107140631 A 20181115; TW 112119907 A 20181115; US 201816764056 A 20181115; US 202217862142 A 20220711; US 202318377016 A 20231005