Title (en)

PROCESSOR ARCHITECTURES

Title (de)

PROZESSORARCHITEKTUREN

Title (fr)

ARCHITECTURES DE PROCESSEUR

Publication

EP 3724779 A1 20201021 (FR)

Application

EP 18833085 A 20181127

Priority

- FR 1762068 A 20171213
- FR 2018052995 W 20181127

Abstract (en)

[origin: WO2019115902A1] A processor (1) comprising a control unit (3) and a plurality of processing units (5) interacting in accordance with an operating architecture, imposed dynamically by the control unit, from among at least two of the following architectures and combinations of the following architectures: - a single instruction stream multiple data stream architecture (SIMD), - a multiple instruction stream single data stream architecture (MISD), - a multiple instruction stream multiple data stream architecture (MIMD). The operating architecture is imposed dynamically by the control unit in accordance with: - configuration functions contained in a machine code and/or - data to be processed and current processing instructions received at the input of the processor.

IPC 8 full level

G06F 15/78 (2006.01)

CPC (source: EP KR US)

G06F 8/41 (2013.01 - KR); **G06F 8/447** (2013.01 - US); **G06F 8/47** (2013.01 - US); **G06F 9/44589** (2013.01 - US); **G06F 15/7871** (2013.01 - EP KR); **G06F 15/80** (2013.01 - US)

Citation (search report)

See references of WO 2019115902A1

Designated contracting state (EPC)

AL AT BE BG CH CY CZ DE DK EE ES FI FR GB GR HR HU IE IS IT LI LT LU LV MC MK MT NL NO PL PT RO RS SE SI SK SM TR

Designated extension state (EPC)

BA ME

DOCDB simple family (publication)

FR 3074931 A1 20190614; **FR 3074931 B1 20200103**; CN 111512296 A 20200807; EP 3724779 A1 20201021; KR 20200121788 A 20201026; US 2021173809 A1 20210610; WO 2019115902 A1 20190620

DOCDB simple family (application)

FR 1762068 A 20171213; CN 201880080771 A 20181127; EP 18833085 A 20181127; FR 2018052995 W 20181127; KR 20207020211 A 20181127; US 201816771376 A 20181127