Title (en)

REGISTER FOR AT-SPEED SCAN TESTING

Title (de)

REGISTER FÜR BEI GESCHWINDIGKEIT DURCHGEFÜHRTEM SCAN-TEST

Title (fr)

REGISTRE PAR TEST DE BALAYAGE RÉALISÉ À VITESSE D'OPÉRATION

Publication

EP 3751298 A1 20201216 (EN)

Application

EP 20177989 A 20200603

Priority

US 201916435531 A 20190609

Abstract (en)

An integrated circuit (IC) has scan chains of stitched registers that support scan testing of functional logic. The scan testing has a shift phase in which incoming and outgoing data are shifted into and out of the registers using a slow clock and a capture phase in which outgoing data from the functional logic is captured by the registers using launch-and-capture pulses of a fast clock to check for delay faults. During a warm-up period after termination of the slow clock but before application of the launch-and-capture pulses, the registers propagate data through their master latches without affecting the data stored in their slave latches. A warm-up controller configures the registers and generates control signals to perform either launch-on-shift or launch-on-capture scan testing. The flow of data and the warm-up controller operations keep the power supply rail voltage sufficiently charged for the fast launch-and-capture pulses.

IPC 8 full level

G01R 31/3185 (2006.01)

CPC (source: EP US)

G01R 31/31725 (2013.01 - US); **G01R 31/3177** (2013.01 - US); **G01R 31/318541** (2013.01 - EP); **G11C 19/28** (2013.01 - US)

Citation (search report)

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- [XI] US 2018059178 A1 20180301 - WANG LING [CN], et al
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Designated contracting state (EPC)

AL AT BE BG CH CY CZ DE DK EE ES FI FR GB GR HR HU IE IS IT LI LT LU LV MC MK MT NL NO PL PT RO RS SE SI SK SM TR

Designated extension state (EPC)

BA ME

DOCDB simple family (publication)

EP 3751298 A1 20201216; US 10948538 B2 20210316; US 2020386808 A1 20201210

DOCDB simple family (application)

EP 20177989 A 20200603; US 201916435531 A 20190609