Title (en)

MIMD PROCESSOR EMULATED ON SIMD ARCHITECTURE

Title (de)

AUF SIMD-ARCHITEKTUR EMULIERTER MIMD-PROZESSOR

Title (fr)

PROCESSEUR MIMD ÉMULÉ SUR ARCHITECTURE SIMD

Publication

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Application

EP 19742845 A 20190606

Priority

- FR 1855012 A 20180608
- FR 2019051352 W 20190606

Abstract (en)

[origin: WO2019234359A1] The present invention relates to a processor having a SIMD architecture, comprising an array (120) of elementary processors (150), each elementary processor (150) being associated with an elementary memory cell (155), a central controller (110) connected to the elementary processors by an instruction bus and a status bus. The central controller transmits a sequence of instructions in a loop, each instruction comprising a calculation flow indicator. Each elementary processor has an instruction filter that makes it possible to reject or take into account an instruction depending on the identifier it contains. This operating mode makes it possible to emulate a MIMD processor on a SIMD architecture.

IPC 8 full level

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CPC (source: EP US)

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