Title (en)

MEMORY ORGANIZATION FOR MATRIX PROCESSING

Title (de)

SPEICHERORGANISATION FÜR MATRIXVERARBEITUNG

Title (fr)

ORGANISATION DE MÉMOIRE POUR TRAITEMENT DE MATRICE

Publication

EP 3798927 A1 20210331 (EN)

Application

EP 20197636 A 20200923

Priority

US 201916588859 A 20190930

Abstract (en)

A system comprises a memory, a plurality of memory banks, and an organizer. The memory is configured to store elements of a matrix, wherein the elements are distributed into overlapping subgroups and each shares at least one element of the matrix with another overlapping subgroup. The plurality of memory banks is configured to store the overlapping subgroups, wherein the subgroups are distributed among the memory banks using a circular shifted pattern. The organizer is configured to read specific ones of the overlapping subgroups in the plurality of memory banks in a specified pattern associated with transposing the matrix.

IPC 8 full level

G06N 3/04 (2006.01); **G06F 17/15** (2006.01); **G06N 3/063** (2006.01); **G06T 1/60** (2006.01)

CPC (source: CN EP US)

G06F 7/468 (2013.01 - EP); **G06F 9/3001** (2013.01 - CN EP US); **G06F 9/30036** (2013.01 - CN EP); **G06F 9/30038** (2023.08 - CN EP); **G06F 12/0207** (2013.01 - EP); **G06F 12/0646** (2013.01 - US); **G06F 17/153** (2013.01 - EP US); **G06F 17/16** (2013.01 - CN US); **G06N 3/045** (2023.01 - EP); **G06N 3/063** (2013.01 - CN EP); **G06N 20/00** (2019.01 - US); G06F 2207/4824 (2013.01 - EP); G06F 2212/1016 (2013.01 - EP US)

Citation (search report)

- [I] US 2016062947 A1 20160303 - CHETLUR SHARANYAN [US], et al
- [I] SHARAN CHETLUR ET AL: "cuDNN: efficient primitives for deep learning", ARXIV:1410.0759V3, 18 October 2014 (2014-10-18), XP055260407, Retrieved from the Internet <URL:http://arxiv.org/abs/1410.0759v3> [retrieved on 20160322]
- [A] JING CHANG ET AL: "An efficient implementation of 2D convolution in CNN", IEICE ELECTRONICS EXPRESS, vol. 14, no. 1, 2017, pages 20161134 - 20161134, XP055762161, DOI: 10.1587/elex.13.20161134
- [A] AHMAD SHAWAHNA ET AL: "FPGA-based Accelerators of Deep Learning Networks for Learning and Classification: A Review", ARXIV.ORG, CORNELL UNIVERSITY LIBRARY, 201 OLIN LIBRARY CORNELL UNIVERSITY ITHACA, NY 14853, 28 December 2018 (2018-12-28), XP081010484, DOI: 10.1109/ACCESS.2018.2890150

Designated contracting state (EPC)

AL AT BE BG CH CY CZ DE DK EE ES FI FR GB GR HR HU IE IS IT LI LT LU LV MC MK MT NL NO PL PT RO RS SE SI SK SM TR

Designated extension state (EPC)

BA ME

DOCDB simple family (publication)

US 10872038 B1 20201222; CN 112580791 A 20210330; EP 3798927 A1 20210331

DOCDB simple family (application)

US 201916588859 A 20190930; CN 202011062908 A 20200930; EP 20197636 A 20200923