

Title (en)
ASYNCHRONOUS PROCESSOR ARCHITECTURE

Title (de)
ARCHITEKTUR EINES ASYNCHRONEN PROZESSORS

Title (fr)
ARCHITECTURE DE PROCESSEUR ASYNCHRONE

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Application
EP 19737810 A 20190521

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Abstract (en)
[origin: WO2020002783A1] The invention concerns a data processing method comprising: - a control unit, at least one ALU (9), a set of registers (11), a memory (13) and a memory interface (15). The method comprises: a) obtaining (101, 102) the memory addresses of the operands; b) reading (103, 104) the operands in the memory (13); c) transmitting (105) an instruction to execute calculations to the ALU (9) without an addressing instruction; d) executing all the elementary operations (106) by the ALU (9) receiving as input each of the operands from the registers (11); e) storing (107) the data forming results of the processing operation on the registers (11); f) obtaining (108) a memory address for each of the data items forming a result of the processing operation; g) writing (109) the results in the memory (13), for storage and via the memory interface (15), by means of the obtained memory addresses.

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