

Title (en)
GROUP III-NITRIDE HIGH-ELECTRON MOBILITY TRANSISTORS WITH BURIED P-TYPE LAYERS AND PROCESS FOR MAKING THE SAME

Title (de)
GRUPPE-III-NITRID-TRANSISTOREN MIT HOHER ELEKTRONENBEWEGLICHKEIT MIT VERGRABENEN P-SCHICHTEN UND VERFAHREN ZU DEREN HERSTELLUNG

Title (fr)
TRANSISTORS À MOBILITÉ D'ÉLECTRONS ÉLEVÉE AU NITRURE DU GROUPE III AVEC COUCHES DE TYPE P ENFOUIES ET LEUR PROCÉDÉ DE FABRICATION

Publication
EP 3918636 A4 20230308 (EN)

Application
EP 20749178 A 20200128

Priority
• US 201916260095 A 20190128
• US 201916376596 A 20190405
• US 2020015331 W 20200128

Abstract (en)
[origin: WO2020159934A1] An apparatus includes a substrate. The apparatus further includes a group III-nitride buffer layer on the substrate; a group III-nitride barrier layer on the group III-nitride buffer layer, the group III-nitride barrier layer including a higher bandgap than a bandgap of the group III-nitride buffer layer. The apparatus further includes a source electrically coupled to the group III-nitride barrier layer; a gate electrically coupled to the group III-nitride barrier layer; a drain electrically coupled to the group III-nitride barrier layer; and a p-region being at least one of the following: in the substrate or on the substrate below said group III-nitride barrier layer.

IPC 8 full level
H01L 29/778 (2006.01); **H01L 29/10** (2006.01); **H01L 29/40** (2006.01); **H01L 29/423** (2006.01); **H01L 29/08** (2006.01); **H01L 29/167** (2006.01); **H01L 29/20** (2006.01); **H01L 29/417** (2006.01)

CPC (source: EP KR)
H01L 29/1075 (2013.01 - EP KR); **H01L 29/2003** (2013.01 - KR); **H01L 29/402** (2013.01 - KR); **H01L 29/423** (2013.01 - EP); **H01L 29/66462** (2013.01 - KR); **H01L 29/7783** (2013.01 - EP); **H01L 29/7787** (2013.01 - EP KR); **H01L 29/0843** (2013.01 - EP); **H01L 29/167** (2013.01 - EP); **H01L 29/2003** (2013.01 - EP); **H01L 29/402** (2013.01 - EP); **H01L 29/41766** (2013.01 - EP); **H01L 29/8124** (2013.01 - EP)

Citation (search report)
• [X] EP 3276670 A1 20180131 - RENESAS ELECTRONICS CORP [JP]
• [X] US 2017365702 A1 20171221 - PRECHTL GERHARD [AT], et al
• [X] US 2013062671 A1 20130314 - SAITO WATARU [JP], et al
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• [X] CHIU HSIEN-CHIN ET AL: "Analysis of the Back-Gate Effect in Normally OFF p-GaN Gate High-Electron Mobility Transistor", IEEE TRANSACTIONS ON ELECTRON DEVICES, IEEE, USA, vol. 62, no. 2, February 2015 (2015-02-01), pages 507 - 511, XP011570701, ISSN: 0018-9383, [retrieved on 20150120], DOI: 10.1109/TED.2014.2377747
• See also references of WO 2020159934A1

Designated contracting state (EPC)
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DOCDB simple family (publication)
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DOCDB simple family (application)
US 2020015331 W 20200128; CN 202080025271 A 20200128; CN 202410377963 A 20200128; EP 20749178 A 20200128; JP 2021544206 A 20200128; JP 2023000240 A 20230104; KR 20217027530 A 20200128; KR 20237004563 A 20200128; KR 20247001387 A 20200128