Title (en)

FERROELECTRIC MEMORY DEVICE CONTAINING WORD LINES AND PASS GATES AND METHOD OF FORMING THE SAME

Title (de)

FERROELEKTRISCHE SPEICHERANORDNUNG MIT WORTLEITUNGEN UND DURCHLASSGATES UND VERFAHREN ZU DEREN HERSTELLUNG

Title (fr)

DISPOSITIF DE MÉMOIRE FERROÉLECTRIQUE CONTENANT DES LIGNES DE MOTS ET DES GRILLES DE PASSAGE ET SON PROCÉDÉ DE FORMATION

Publication

EP 3991205 A4 20230712 (EN)

Application

EP 19934652 A 20191230

Priority

- US 201916457687 A 20190628
- US 201916457721 A 20190628
- US 2019068871 W 20191230

Abstract (en)

[origin: WO2020263339A1] A memory device includes a semiconductor channel extending between a source region and a drain region, a plurality of pass gate electrodes, a plurality of word lines, a gate dielectric located between the semiconductor channel and the plurality of pass gate electrodes, and ferroelectric material portions located between the semiconductor channel and the plurality of word lines

IPC 8 full level

H01L 21/28 (2006.01); **G11C 11/22** (2006.01); **H01L 29/78** (2006.01); **H10B 51/20** (2023.01); **H10B 51/30** (2023.01)

CPC (source: EP KR)

G11C 11/223 (2013.01 - EP KR); **G11C 11/2259** (2013.01 - EP KR); **H10B 51/20** (2023.02 - EP KR); **H10B 51/30** (2023.02 - EP KR)

Citation (search report)

- [XAI] US 2017278858 A1 20170928 - WALKER ANDREW J [US], et al
- [IA] US 2017148805 A1 20170525 - NISHIKAWA MASATOSHI [JP], et al
- [IA] US 8173533 B2 20120508 - KIM JINGYUN [KR], et al
- [A] US 2015357413 A1 20151210 - ZHANG YANLI [US], et al
- [A] FLORENT K ET AL: "First demonstration of vertically stacked ferroelectric Al doped HfO2 devices for NAND applications", 2017 SYMPOSIUM ON VLSI TECHNOLOGY, JSAP, 5 June 2017 (2017-06-05), XP033135080, DOI: 10.23919/VLSIT.2017.7998162
- See also references of WO 2020263339A1

Designated contracting state (EPC)

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DOCDB simple family (publication)

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DOCDB simple family (application)

US 2019068871 W 20191230; CN 201980078936 A 20191230; EP 19934652 A 20191230; KR 20217019754 A 20191230; KR 20237017845 A 20191230