Title (en)

MULTI-PHASE TOPOLOGY SYNTHESIS OF A NETWORK-ON-CHIP (NOC)

Title (de)

MEHRPHASIGE TOPOLOGIESYNTHESE EINES NETZWERKS AUF EINEM CHIP (NOC)

Title (fr)

SYNTHÈSE DE TOPOLOGIE MULTIPHASE D'UN RÉSEAU SUR PUCE (NOC)

Publication

EP 4013014 A1 20220615 (EN)

Application

EP 21204156 A 20211022

Priority

US 202017116344 A 20201209

Abstract (en)

A process is disclosed that automatically creates a network-on-chip (NoC) very quickly using a set of constraints, which are requirements for the NoC. The process takes a set of constraints as inputs and produces a NoC with all its elements configured and a placement of such elements on the floorplan of the chip.

IPC 8 full level

H04L 41/14 (2022.01)

CPC (source: CN EP)

G06F 15/7825 (2013.01 - CN); **H04L 41/145** (2013.01 - EP)

Citation (search report)

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Designated contracting state (EPC)

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Designated extension state (EPC)

BA ME

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