

Title (en)  
LEAKAGE COMPENSATION DYNAMIC REGISTER, DATA COMPUTING UNIT, CHIP, COMPUTING POWER BOARD, AND COMPUTING APPARATUS

Title (de)  
DYNAMISCHES LEAKAGEKOMPENSATIONSREGISTER, DATENBERECHNUNGSEINHEIT, CHIP, RECHNERNETZPLATINE UND RECHNERGERÄT

Title (fr)  
REGISTRE DYNAMIQUE DE COMPENSATION DE FUITE, UNITÉ DE CALCUL DE DONNÉES, PUCE, CARTE DE PUISSANCE INFORMATIQUE ET APPAREIL INFORMATIQUE

Publication  
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Application  
**EP 20871371 A 20200629**

Priority  
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Abstract (en)  
[origin: EP4040440A1] The invention provides a leakage compensation dynamic register, a data operation unit, a chip, a hash board, and a computing apparatus. The leakage compensation dynamic register comprises: an input terminal, an output terminal, a clock signal terminal, and an analog switch unit; a data latch unit for latching the data under control of the clock signal; and an output drive unit for inverting and outputting the data received from the data latch unit, the analog switch unit, the data latch unit, and the output drive unit being sequentially connected in series between the input terminal and the output terminal, and the analog switch unit and the data latch unit having a node therebetween, wherein the leakage compensation dynamic register further comprises a leakage compensation unit electrically connected between the node and the output terminal. The invention can effectively compensate for a dynamic leakage current of the node, thereby improving data security and accuracy.

IPC 8 full level  
**G11C 19/28** (2006.01); **G06F 15/78** (2006.01); **H03K 3/356** (2006.01)

CPC (source: CN EP KR US)  
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Citation (search report)  
• [XAYI] US 4896296 A 19900123 - TURNER JOHN E [US], et al  
• [XAYI] US 5929687 A 19990727 - YAMAUCHI HIROYUKI [JP]  
• [XAYI] US 8115531 B1 20120214 - BROWN JEFF S [US], et al  
• See also references of WO 2021063052A1

Designated contracting state (EPC)  
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