

Title (en)  
SYSTEMS, APPARATUSES, AND METHODS FOR FUSED MULTIPLY ADD

Title (de)  
SYSTEME, VORRICHTUNGEN UND VERFAHREN FÜR FUSIONIERTE MULTIPLIKATIONSADDITION

Title (fr)  
SYSTÈMES, APPAREILS ET PROCÉDÉS POUR ADDITION-MULTIPLICATION FUSIONNÉES

Publication  
**EP 4148563 A1 20230315 (EN)**

Application  
**EP 22203441 A 20161020**

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• US 2016057991 W 20161020

Abstract (en)  
In some embodiments, an apparatus with execution circuitry is provided. The execution circuitry is to execute a single instruction to, for each result packed data element: preserve an existing value of the result packed data element or set the result packed data element to zero if a corresponding bit value in a writemask register is set to a first value; and if the corresponding bit value in the writemask register is set to a second value, then: multiply a first number of a first source packed data elements with corresponding packed data elements of a second source packed data elements to produce a first number of products, add the first number of products to a corresponding packed data element from a third source packed data elements to produce the result packed data element of a second size in a corresponding position in a source/destination packed data register.

IPC 8 full level  
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CPC (source: CN EP US)  
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Citation (search report)  
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Citation (examination)  
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