Title (en)

VARIATION TOLERANT LATCH-BASED CLOCKING

Title (de)

VARIATIONSTOLERANTE LATCH-BASIERTE TAKTUNG

Title (fr)

CRÉATION D'HORLOGE BASÉE SUR UN VERROU TOLÉRANT AUX VARIATIONS

Publication

EP 4241382 A1 20230913 (EN)

Application

EP 21889982 A 20211103

Priority

- US 202063110274 P 20201105
- US 2021057890 W 20211103

Abstract (en)

[origin: WO2022098753A1] A clock pulse suppression logic to generate local non-overlapping 3-phase clock from a globally forwarded clock topology. The digest data path uses a global forwarded clock topology where the 2x frequency clock is forwarded unidirectionally from one pipeline stage to the next. Each pipeline stage implements an all-digital pulse suppression logic using a daisy-chained enable signal to locally generate the 3-phase clocks. An optimized data path is used for both digest and scheduler, where output inversion at each Boolean function and carry-save adder tree are removed, resulting in inverted outputs at each stage. The functional inversions are corrected or accounted for in the subsequent stages of the data path, generating the expected final hash output.

IPC 8 full level

H03K 19/17728 (2020.01); **G06Q 20/06** (2012.01); **H03K 19/17736** (2020.01); **H04L 9/06** (2006.01)

CPC (source: EP)

G06F 1/06 (2013.01); **G09C 1/00** (2013.01); **H04L 9/3239** (2013.01); **H04L 9/50** (2022.05); H03K 19/17728 (2013.01); H03K 19/17736 (2013.01); H04L 2209/12 (2013.01)

Designated contracting state (EPC)

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Designated extension state (EPC)

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