Title (en)

COMPUTE-IN-MEMORY (CIM) BIT CELL CIRCUITS EACH DISPOSED IN AN ORIENTATION OF A CIM BIT CELL CIRCUIT LAYOUT INCLUDING A READ WORD LINE (RWL) CIRCUIT IN A CIM BIT CELL ARRAY CIRCUIT

Title (de)

RECHEN-IN-SPEICHER (CIM)-BITZELLENSCHALTUNGEN MIT JEWEILS EINER AUSRICHTUNG EINER CIM-BITZELLENSCHALTUNGSLAYOUT MIT EINER LESEWORTLEITUNG (RWL)-SCHALTUNG IN EINER CIM-BITZELLENANORDNUNG

Title (fr)

CIRCUITS DE CELLULE BINAIRE DE CALCUL EN MÉMOIRE (CIM) PLACÉS CHACUN DANS UNE ORIENTATION D'UN AGENCEMENT DE CIRCUIT DE CELLULE BINAIRE CIM COMPRENANT UN CIRCUIT DE LIGNE DE MOTS DE LECTURE (RWL) DANS UN CIRCUIT DE RÉSEAU DE CELLULES BINAIRES CIM

Publication

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Application

EP 21801308 A 20210930

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Abstract (en)

[origin: WO2022119627A1] Compute-in-memory (CIM) bit cell array circuits include CIM bit cell circuits for multiply-accumulate operations. The CIM bit cell circuits include a memory bit cell circuit for storing a weight data in true and complement form. The CIM bit cell circuits include a true pass-gate circuit and a complement pass-gate circuit for generating a binary product of the weight data and an activation input on a product node. An RWL circuit couples the product node to a ground voltage for initialization. The CIM bit cell circuits also include a plurality of consecutive gates each coupled to at least one of the memory bit cell circuit, the true pass-gate circuit, the complement pass-gate circuit, and the RWL circuit. Each of the CIM bit cell circuits in the CIM bit cell array circuit is disposed in an orientation of a CIM bit cell circuit layout including the RWL circuit.

IPC 8 full level

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CPC (source: EP)

G11C 5/025 (2013.01); **G11C 7/1006** (2013.01); **G11C 11/54** (2013.01); **H01L 27/0207** (2013.01); **H10B 10/12** (2023.02); G11C 11/4096 (2013.01)

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