Title (en)

CALIBRATION OF DIGITAL-TO-ANALOG CONVERTERS

Title (de)

KALIBRIERUNG VON DIGITAL-ANALOG-WANDLERN

Title (fr)

ÉTALONNAGE DE CONVERTISSEURS NUMÉRIQUE-ANALOGIQUE

Publication

EP 4258553 A1 20231011 (EN)

Application

EP 23158077 A 20230222

Priority

- US 202263314614 P 20220228
- US 202318171197 A 20230217

Abstract (en)

Techniques that enable calibration of digital-to-analog Converters (DACs) with minimal processing overhead. A single frequency bin can be used to calibrate errors between bits. A low frequency feedback path can be included into a low frequency low power ADC to determine the error signal that exists in the calibration bin. The bits are calibrated when this error signal is minimized. The calibration techniques described provide an extremely efficient and optimal calibration at the DAC output of both static and dynamic errors.

IPC 8 full level

H03M 1/10 (2006.01); H03M 1/66 (2006.01)

CPC (source: EP KR US)

H03M 1/1004 (2013.01 - EP KR); **H03M 1/1009** (2013.01 - US); **H03M 1/1023** (2013.01 - KR); **H03M 1/1095** (2013.01 - EP); **H03M 1/661** (2013.01 - KR); H03M 1/66 (2013.01 - EP)

Citation (applicant)

US 201462633146 P

Citation (search report)

- [XI] EP 3242404 A1 20171108 - ANALOG DEVICES INC [US]
- [A] US 2021194492 A1 20210624 - ZHAO JIALIN [CN], et al

Designated contracting state (EPC)

AL AT BE BG CH CY CZ DE DK EE ES FI FR GB GR HR HU IE IS IT LI LT LU LV MC ME MK MT NL NO PL PT RO RS SE SI SK SM TR

Designated extension state (EPC)

BA

Designated validation state (EPC)

KH MA MD TN

DOCDB simple family (publication)

US 2023275596 A1 20230831; EP 4258553 A1 20231011; JP 2023126199 A 20230907; KR 20230128984 A 20230905; TW 202337141 A 20230916

DOCDB simple family (application)

US 202318171197 A 20230217; EP 23158077 A 20230222; JP 2023030239 A 20230228; KR 20230024619 A 20230223; TW 112106921 A 20230224