

Title (en)
NUMERICAL PRECISION IN DIGITAL MULTIPLIER CIRCUITRY

Title (de)
NUMERISCHE PRÄZISION IN DIGITALEN MULTIPLIZIERSCHALTUNGEN

Title (fr)
PRÉCISION NUMÉRIQUE DANS UN ENSEMBLE CIRCUIT MULTIPLICATEUR NUMÉRIQUE

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Application
EP 21918010 A 20210628

Priority

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Abstract (en)
[origin: WO2022150058A1] In one embodiment, multiplier circuitry multiplies operands of a first format. One or more storage register circuits store digital bits corresponding to an operand and another operand of the first format. A decomposing circuit decomposes the operand into a first plurality of operands, and the other operand into a second plurality of operands. Each multiplier circuit multiplies a respective first operand of the first plurality of operands with a respective second operand of the second plurality of operands to generate a corresponding partial result of a plurality of partial results. An accumulator circuit accumulates the plurality of partial results using a second format to generate a complete result of the second format that is stored in the accumulator circuit. A conversion circuit truncates the complete result of the second format and converts the truncated result into an output result of an output format.

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