Title (en)

CIRCUIT ARRANGEMENT FOR VALIDATION OF OPERATION OF A LOGIC MODULE IN A MULTIPOWER LOGIC ARCHITECTURE AND CORRESPONDING VALIDATION METHOD

Title (de)

SCHALTUNGSANORDNUNG ZUR VALIDIERUNG DES BETRIEBS EINES LOGIKMODULS IN EINER LOGISCHEN ARCHITEKTUR MIT MEHREREN LEISTUNGSSTUFEN UND ENTSPRECHENDES VALIDIERUNGSVERFAHREN

Title (fr)

CIRCUIT POUR LA VALIDATION DU FONCTIONNEMENT D'UN MODULE LOGIQUE DANS UNE ARCHITECTURE LOGIQUE À PUISSANCES MULTIPLES ET PROCÉDÉ DE VALIDATION CORRESPONDANT

Publication

EP 4290254 A1 20231213 (EN)

Application

EP 23174170 A 20230518

Priority

IT 202200012056 A 20220607

Abstract (en)

Circuit arrangement for validation of operation of a logic module (11) in a multipower logic architecture (10), comprisingat least a first logic module (11) operating with a first clock signal (MCK) and a first power supply (VMP), anda second logic module (12) operating with a second clock signal (SCK) and second power supply (VMP),said first logic module (11) and second logic module (12) being configured to exchange signals at least on a communication link (DL), whereinthe first logic module (11) is configured to generate a first validation signal (A) and a second validation signal (B), in particular on a first and second wire respectively, which are sent over the communication link (DL) to the second logic module (12), the values of said first validation signal (A) and second validation signal (B) being never zero at the same time,the second logic module (12) being configured toperform a first check that the second validation signal (B) is always logic one when the first validation signal (A) is zero,perform a second check that the first validation signal (A) is always logic one when the second validation signal (B) is zero,perform a cyclic check that the first validation signal (A) and the second validation signal (B) are not stuck-at-1, andto validate (MV) the operation of the first logic module (A) if said first check, second check and cyclic check give each a positive result.

IPC 8 full level

G01R 31/317 (2006.01)

CPC (source: EP US)

G01R 31/31712 (2013.01 - EP); **G01R 31/31721** (2013.01 - EP); **G01R 31/31725** (2013.01 - US); **G01R 31/3177** (2013.01 - US); **G06F 1/08** (2013.01 - US)

Citation (search report)

- [A] US 2015303900 A1 20151022 - WANG PENG [CN], et al
- [A] US 2020132762 A1 20200430 - KUKREJA HIMANSHU [IN], et al
- [A] US 2015186113 A1 20150702 - SKOGLUND PER CARSTEN [NO], et al
- [A] US 2011221502 A1 20110915 - MEIJER RINZE IDA MECHTILDIS PETER [NL], et al

Designated contracting state (EPC)

AL AT BE BG CH CY CZ DE DK EE ES FI FR GB GR HR HU IE IS IT LI LT LU LV MC ME MK MT NL NO PL PT RO RS SE SI SK SM TR

Designated extension state (EPC)

BA

Designated validation state (EPC)

KH MA MD TN

DOCDB simple family (publication)

EP 4290254 A1 20231213; CN 117194115 A 20231208; IT 202200012056 A1 20231207; US 2023393198 A1 20231207

DOCDB simple family (application)

EP 23174170 A 20230518; CN 202310661600 A 20230606; IT 202200012056 A 20220607; US 202318324583 A 20230526