

Title (en)

PARALLEL PROCESSING ARCHITECTURE USING SPECULATIVE ENCODING

Title (de)

PARALLELVERARBEITUNGSARCHITEKTUR MIT SPEKULATIVER KODIERUNG

Title (fr)

ARCHITECTURE DE TRAITEMENT PARALLÈLE UTILISANT UN CODAGE SPÉCULATIF

Publication

EP 4315045 A1 20240207 (EN)

Application

EP 22776686 A 20220325

Priority

- US 202163166298 P 20210326
- US 2022021838 W 20220325

Abstract (en)

[origin: WO2022204450A1] Techniques for program execution in a parallel processing architecture using speculative encoding are disclosed. A two-dimensional array of compute elements is accessed, where each compute element within the array of compute elements is known to a compiler and is coupled to its neighboring compute elements within the array of compute elements. Control for the array of compute elements is provided on a cycle-by-cycle basis. The control is enabled by a stream of wide, variable length, control words generated by the compiler. Two or more operations are coalesced into a control word, where the control word includes a branch decision and operations associated with the branch decision. The coalesced control word includes speculatively encoded operations for at least two possible branch paths. The at least two possible branch paths generate independent side effects. Operations associated with the branch decision that are not indicated by the branch decision are suppressed.

IPC 8 full level

G06F 9/38 (2018.01); **G06F 7/575** (2006.01); **G06F 8/41** (2018.01); **G06F 9/30** (2018.01); **G06F 9/48** (2006.01); **G06F 15/80** (2006.01)

CPC (source: EP KR)

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Designated contracting state (EPC)

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Designated extension state (EPC)

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KH MA MD TN

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